DT system electronics upgrade in context of HL-LHC

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On behalf of the CMS Muon group

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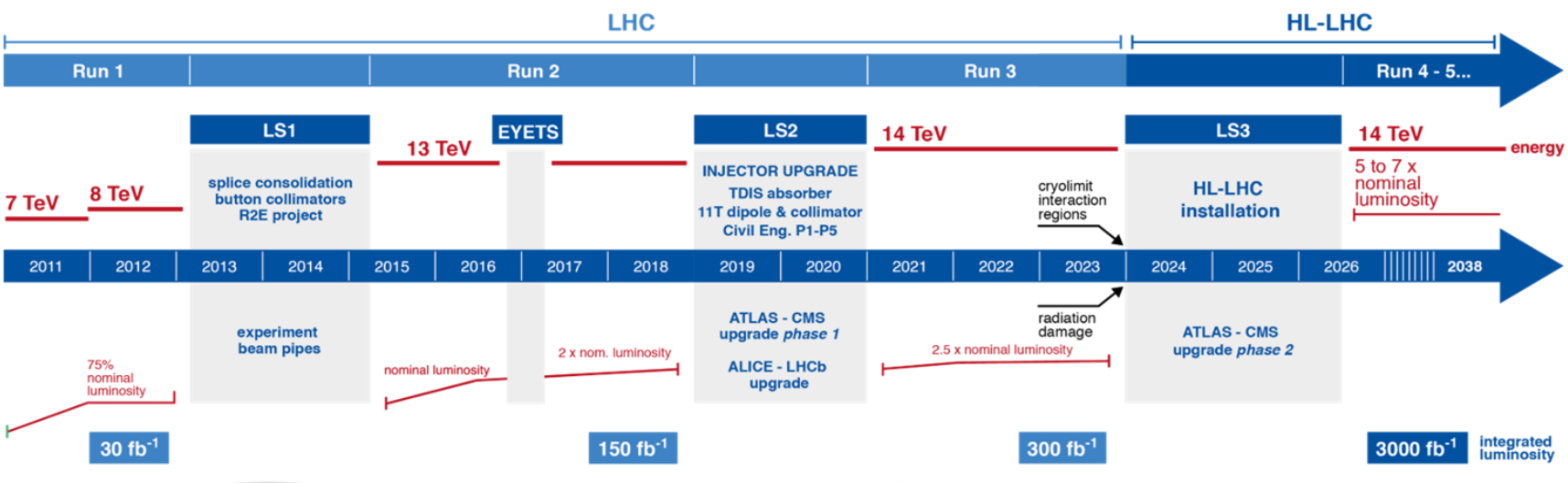
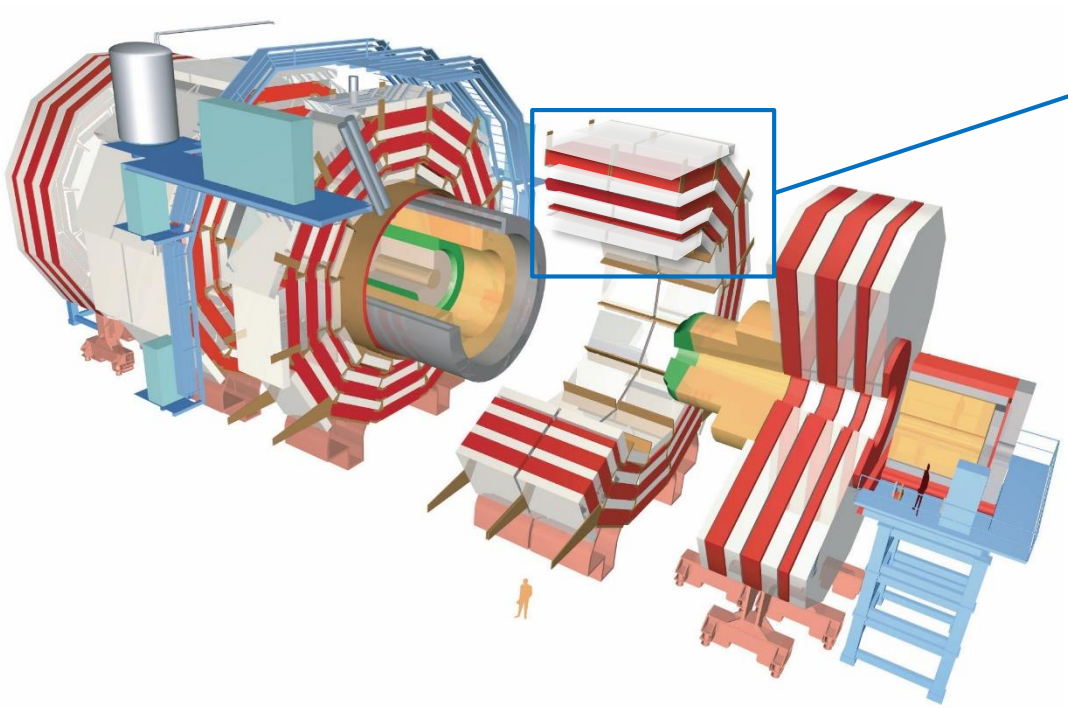
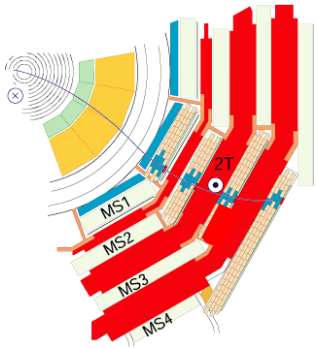
Upgrade activities of DT chamber electronics

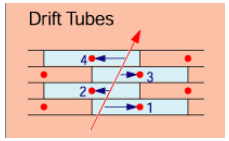


Muon Drift Tubes (DTs) of the CMS detector

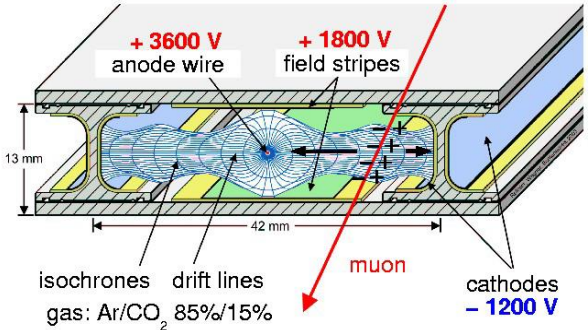


Drift Tubes chambers consist of multiple oblong gas detectors cells





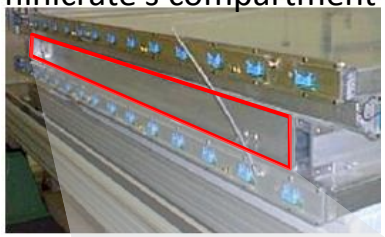
A cut view of an individual cell:



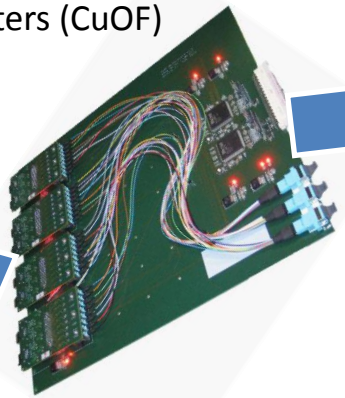
- 700 to 1200 DT cells per chamber
- 172 000 DT cells in the whole CMS

The Legacy Chain: signal path from DT Chamber

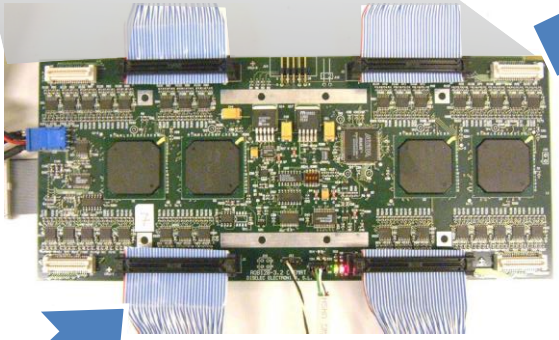
minicrate‘s compartment



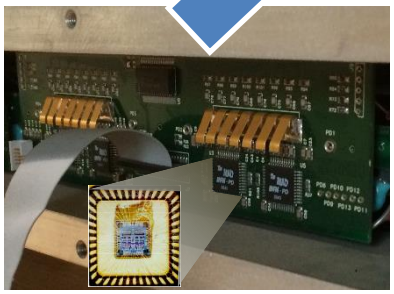
Copper to Optic Fiber converters (CuOF)



uROS and TwinMux boards (uTCA crate)



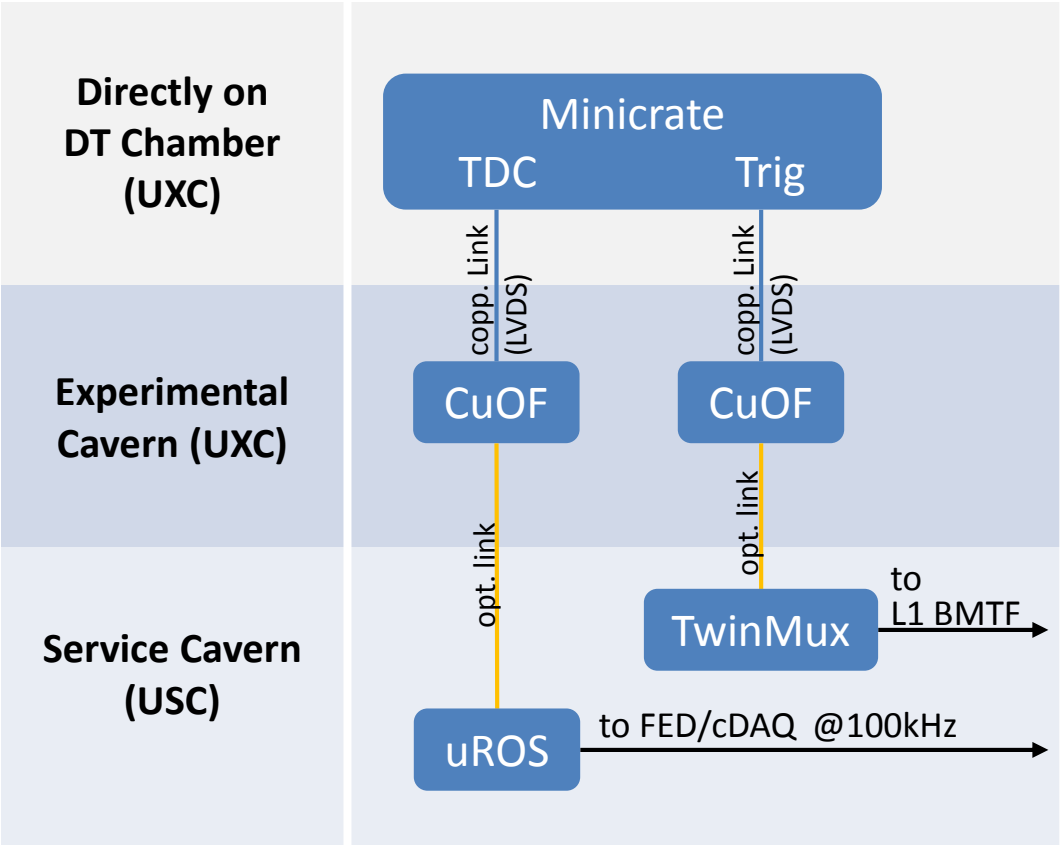
Minicrate Read-out Board (ROB)
the readout of MAD chips
(by the customly designed HPTDC ASICs).



Front-End Board inside the DT Chamber
Heart component - customly designed ASIC „MAD Chip“

Each MAD provides the readout of 4 drift cells
Output: Low Voltage Differential Signal (LVDS)

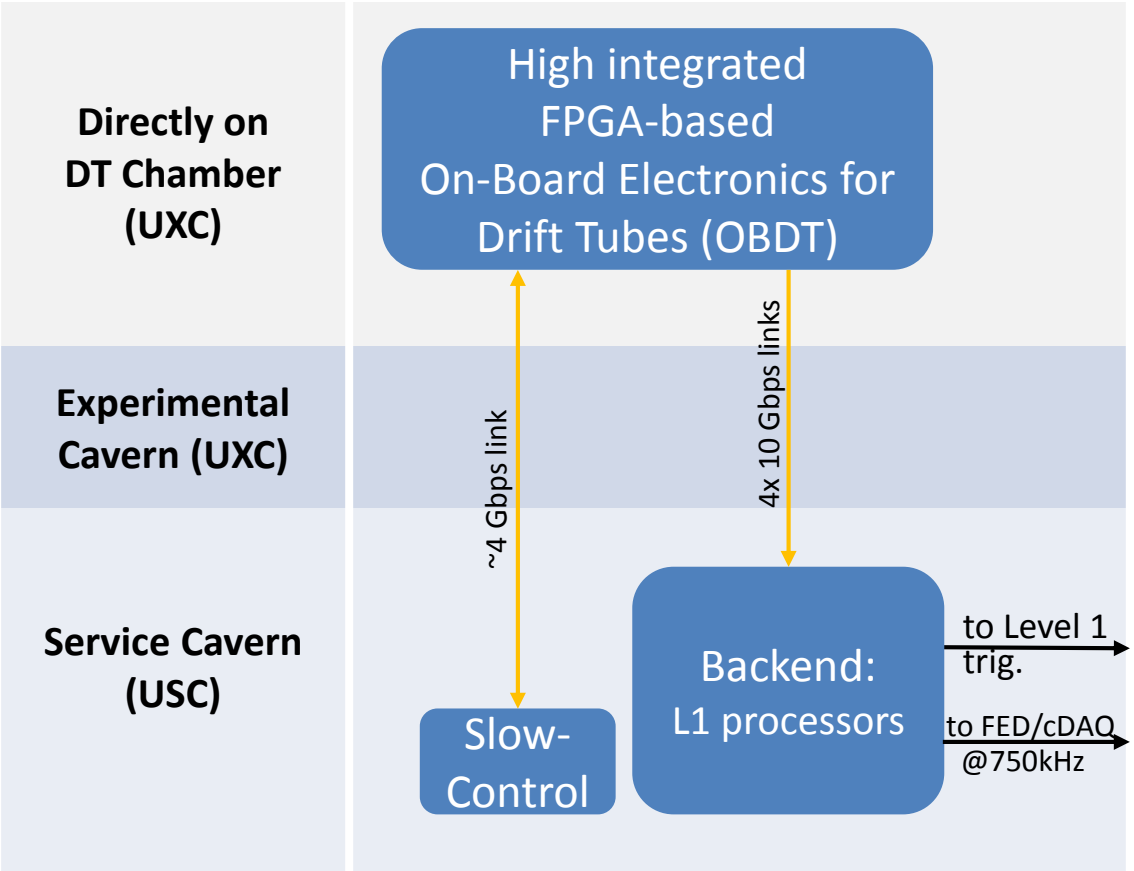
DT electronics current state and upgrade motivation



- Total irradiation doses corresponds to 500 fb^{-1}
- Forced to use the optical translators (CuOFs). However, the less components in UXC – the better
- Not robust against single-hit inefficiency
- Limited to L1 rate of max. 300kHz (but >500kHz is needed!)
- Consists of a lot of different components inside minicrate

Acronyms used: BMTF = Barrel Muon Track Finder; TDC = Time-to-Digital converter

DT electronics Upgrade



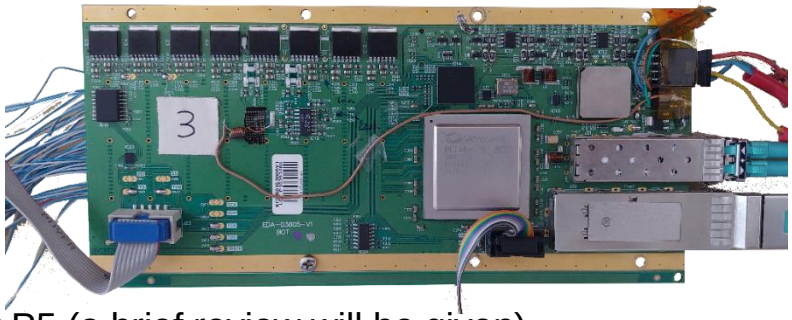
- New generation of the on-chamber electronics:
  - ✓ TDCs (implemented in FPGA)
  - ✓ Slow-control logic (PADC, Temperature, Alignment)
- Rad. tolerant components
- Trigger logic moves completely to the Backend at USC
- Benefits:
  - ✓ Higher L1 rate
  - ✓ Reduced HW complexity
  - ✓ more convinient maintainance
  - ✓ Trigger primitive generation based on the full detector's scope

Acronyms used: TDC = Time-to-Digit Converter; PADC – Pressure ADC

New Minicrate electronics: the OBDT board

Key features

- Central component is PolarFire FPGA (MPF300T) from MicroSemi
- The choosen FPGA is flash based and therefore radiation-tolerant
- TDCs are implemented in FPGA
- 240x TDCs per Board (i.e. 3-4 OBDTs per DT chamber)
- GBT chipset is present: for clock and slow control distribution
- Design ensures readout pipeline
- Buffering and trigger primitive generation to be done outside the experimental cavern



Graphics source: Javier Sastre

Status

- 14x PCB prototypes are ready and assembled
- Data is being taken at the teststand and in slice tests at P5 (a brief review will be given)
- Tests include cosmic data acquisition as well as the test pulses
- Ongoing work for achieving compatibility with some old periphery of DT chambers (implementing a „slow“ I2C)
- A few minor issues of the prototype are documented and will be taken into account by development of the next prototype
- lpGBT chipset to replace the current GBTx chipset

Overview of the current OBDT prototype architecture

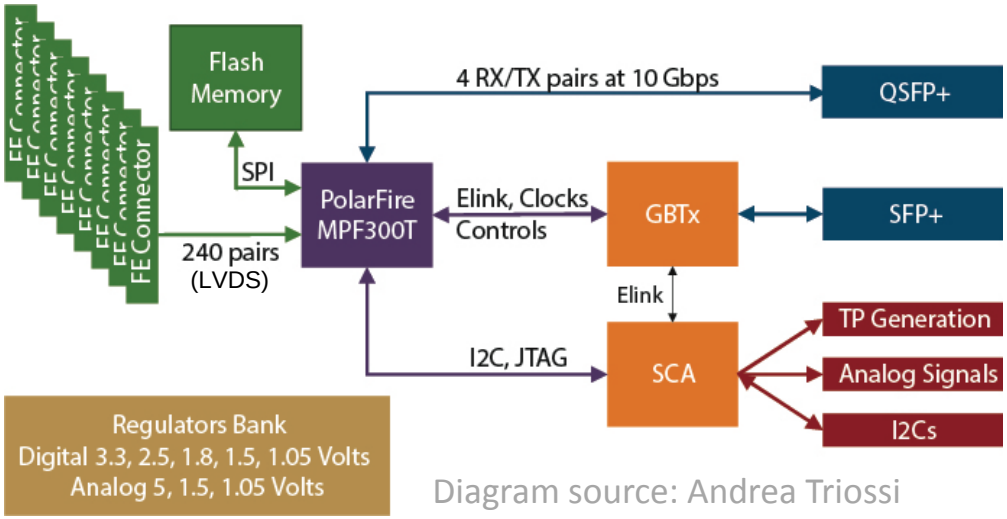


Diagram source: Andrea Triossi

- Readout from the „old“ frontend via LVDS directly to the PolarFire FPGA (8 FE Connectors je. 68 pins)
- Data streaming to backend directly from the PolarFire via optic fibers (GBT protocol)
- GBTx chipset: clock extraction + Slow-control data
- SCA Chip: slow-control ops (Testpulses, Temperature measurements, Sensing of voltage rails)

Development tool for the PolarFire FPGA: Microsemi Libero

OBDT Board communication

OBDT at DT chamber (UXC)

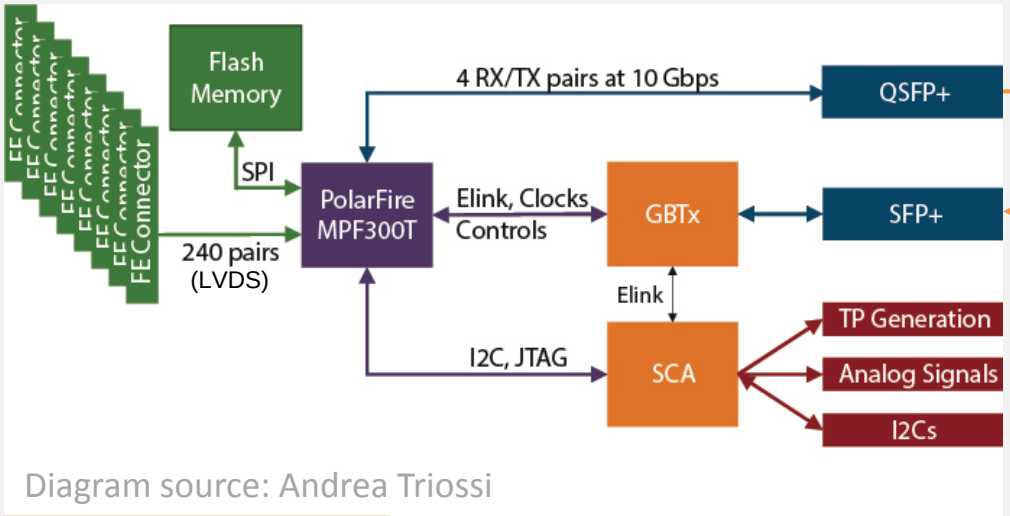


Diagram source: Andrea Triossi

x4
10 Gbps

x1
~4 Gbps

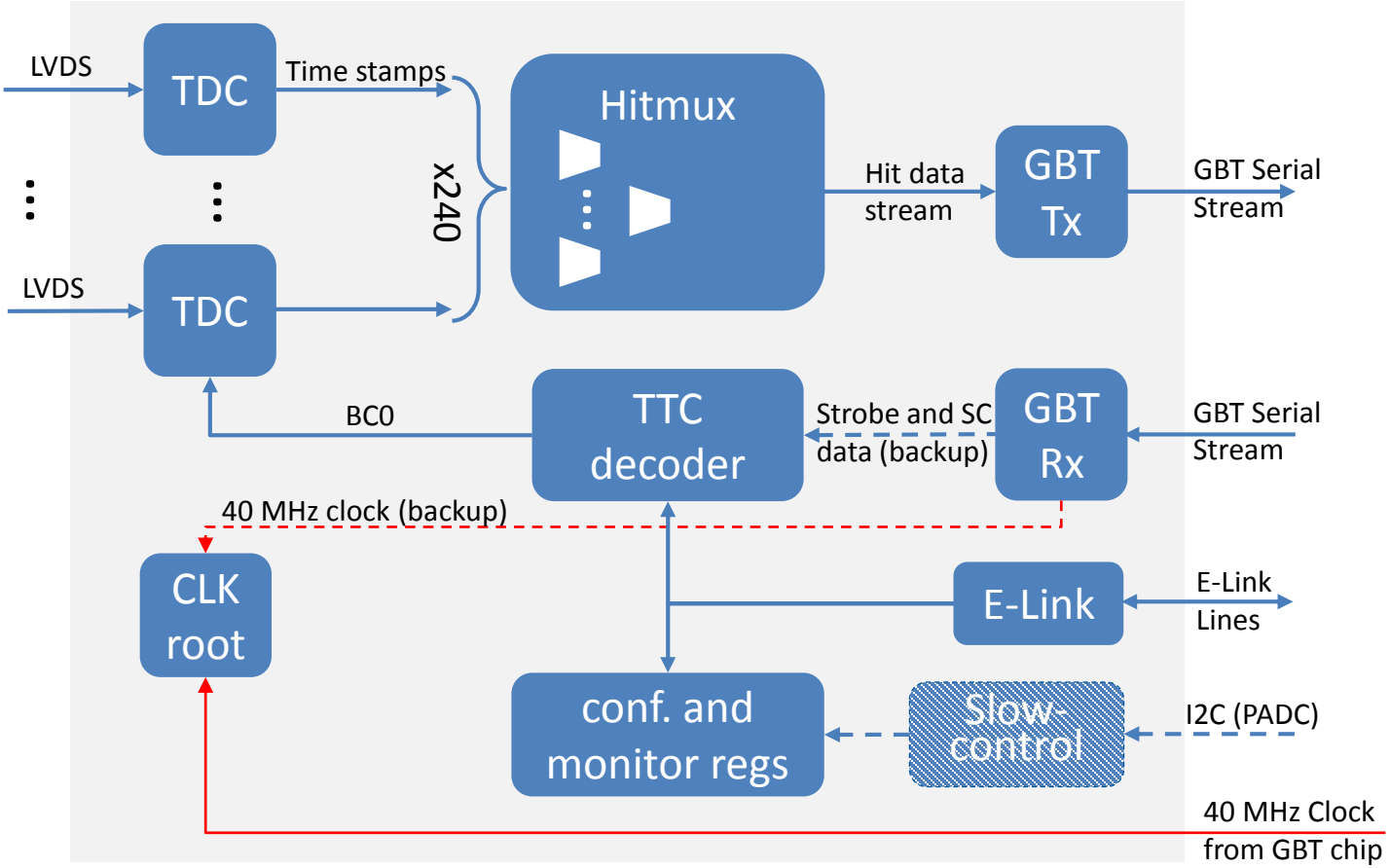
uTCA crate in USC

AB7
(Trigger logic, Interfacing higher-level DAQ)

MoCo
(Slow Control)

- Communication via optics (GBT protocol)
- Both AB7 and MoCo boards are based on the same hardware: TM7
- One AB7 board per DT chamber
- One MoCo controlling up to twelve OBDTs

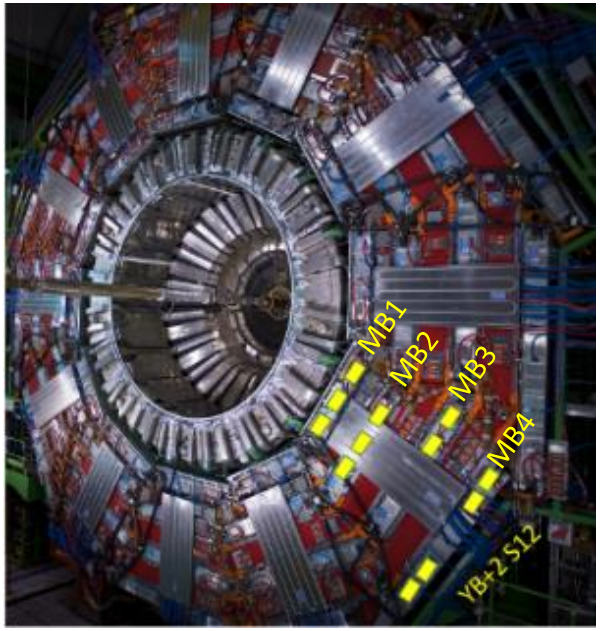
FPGA firmware architecture of OBDT



- TDCs have time-resolution of better than 1ns
- the transfer of hit data is performed directly through fast serializers of the FPGA (up to 10Gbps)

Slice tests at P5

Instrumentation of the Different DT Chambers



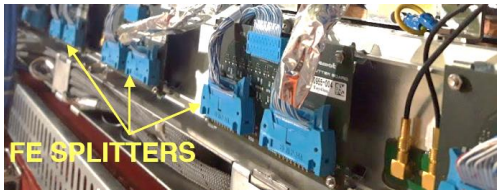
12 OBDT prototypes are mounted in the sector in total

MB1 and MB2

- All possible integration activities are performed here in order to get as close as possible to the final configuration: cooling, mechanics, cabling
- Important purpose here is to obtain the appreciation of the replacement routine for the LS3

MB3 and MB4

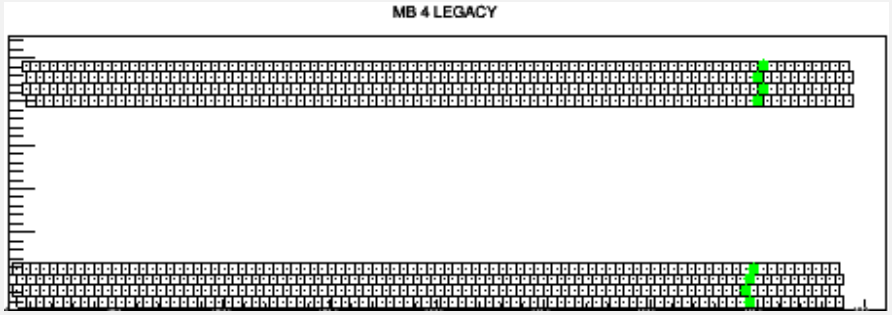
- Work in parallel with the legacy chain (with the Splitters installed directly after the Frontend)
- Purpose is to validate the hits data, which is acquired with the new read-out chain

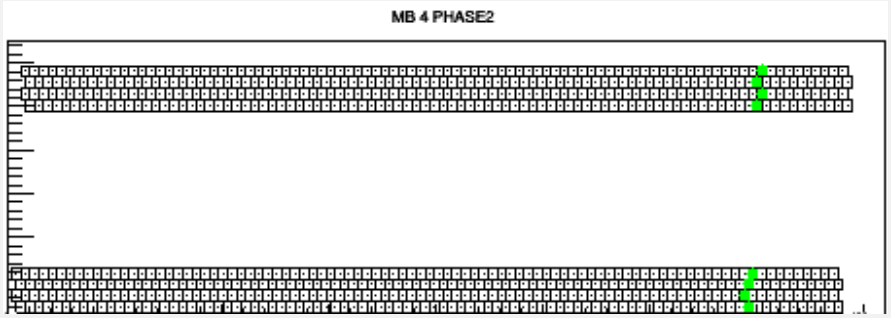


Slice tests results (yet with cosmics)

Spatial coincidence

CMS DT chamber YB+2 S12 MB4 (Run 330675, Event 41).

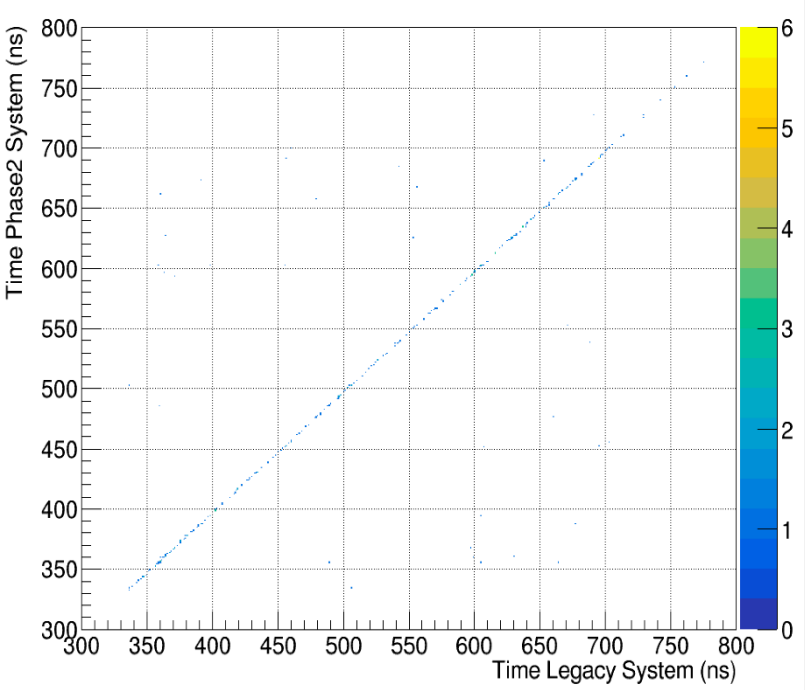




Graphics: Cristina Fernandez Beboya, Alberto Bragagnolo

Time coincidence

Phase 2 vs Legacy time measurement (Run 330848).



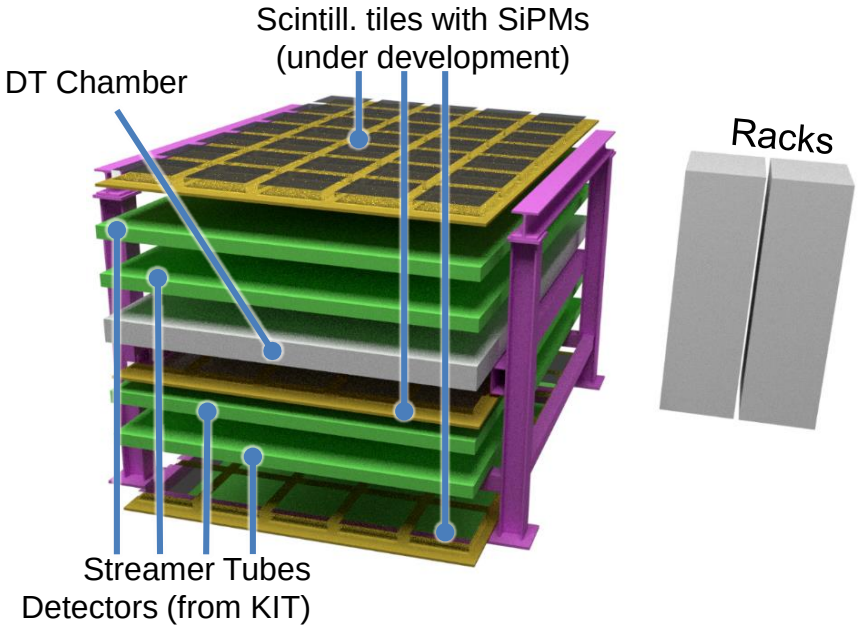
Graphics: Lourdes Urda, Jonas Roemer

*data from three channels (83,86,87), having similar offset within OBDT, was taken for the plot

!!! More results in the talk of Carlo Battilana

Meanwhile in Aachen...
Building up a Cosmic Teststand

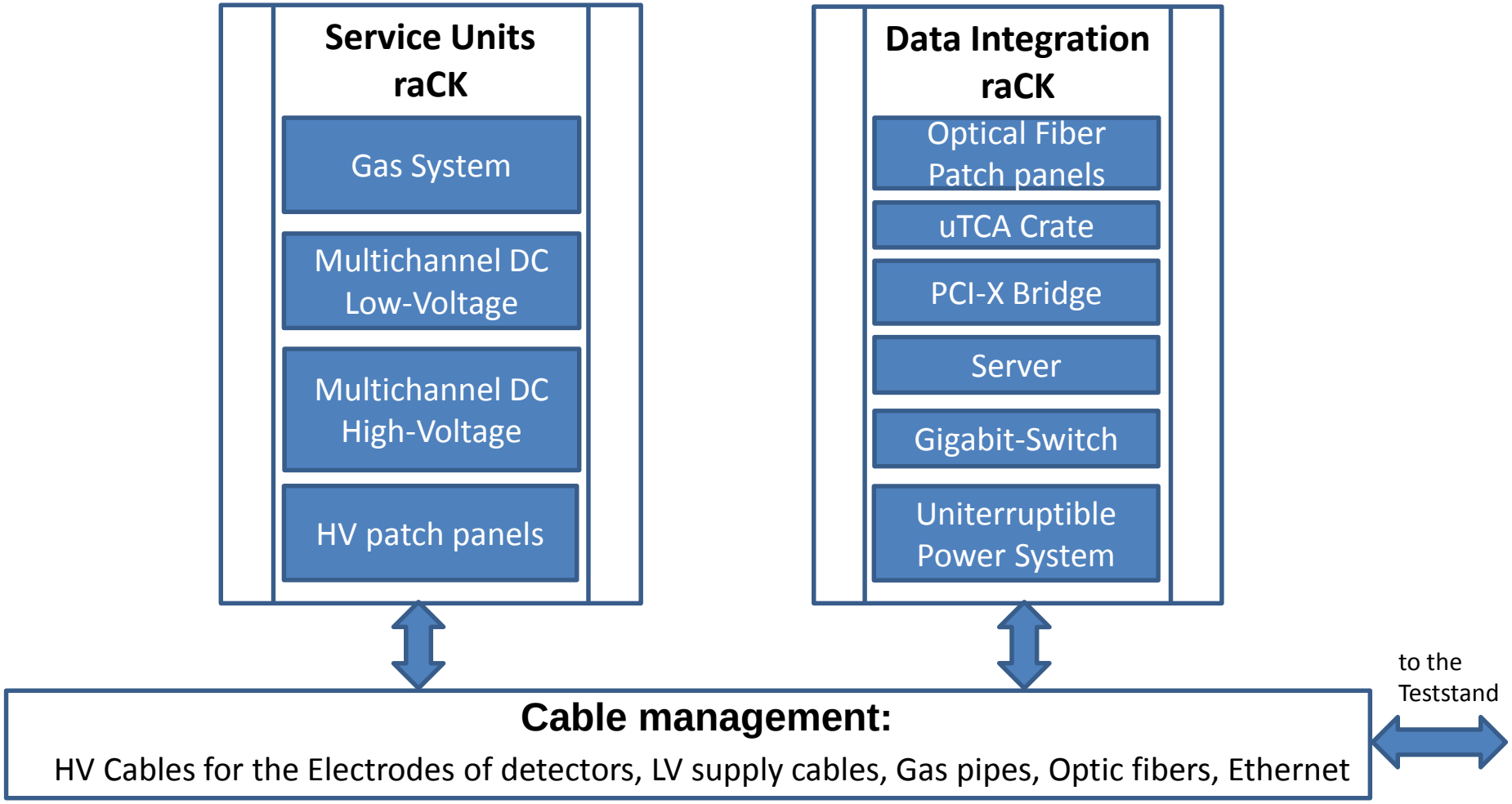
Aachen Cosmic Teststand



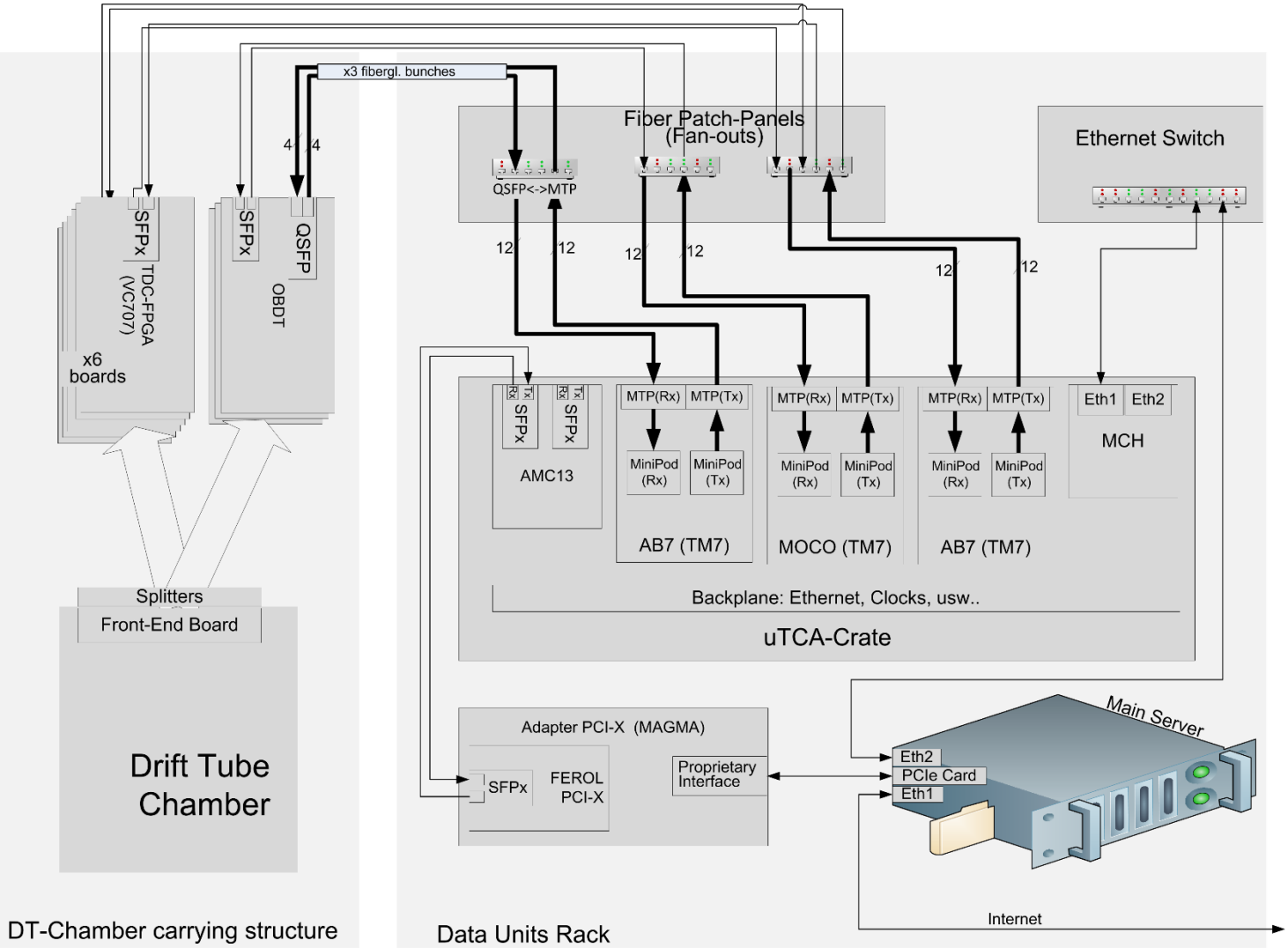
- A fully functioning part of the CMS detector which includes full instrumentation
- Tool for tests and debugging of the new generation DT electronics (running in parallel with CIEMAT and CERN)
- Unique facility for verification of other detectors (GEM, SiPM tiles). Additional layers provide redundancy, which facilitates the verification.

Infrastructure of the Aachen Cosmic Teststand

All units outside the Teststand are distributed between two 19“ racks



Reproducing CMS read-out chain



Summary

- New electronics for DT: better and faster
- First tests at CMS are successful
- Aachener Teststand is being built up - to support the further development and tests of the new DT electronics

Thanks for your attention!

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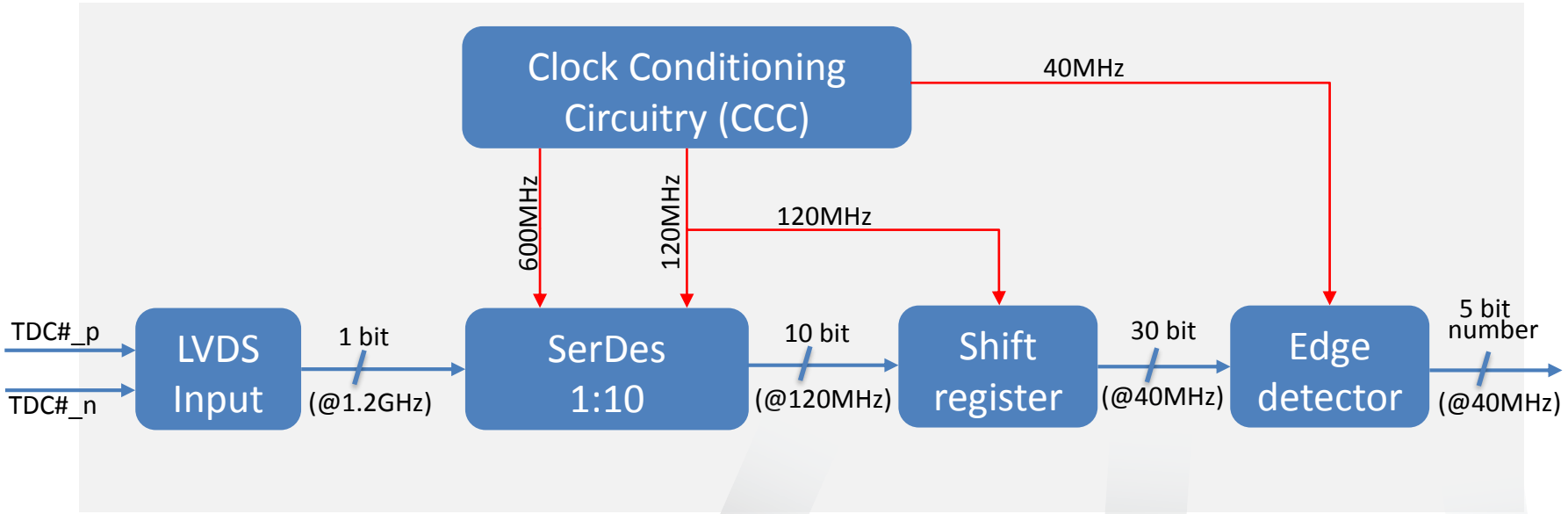
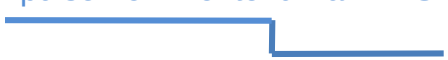
Backup

Implementation of a TDC



Example:

pulse from frontend via LVDS



1. 1111111111
2. 1111111100
3. 0000000000

30'b111111111111111111000000000000

18th bit

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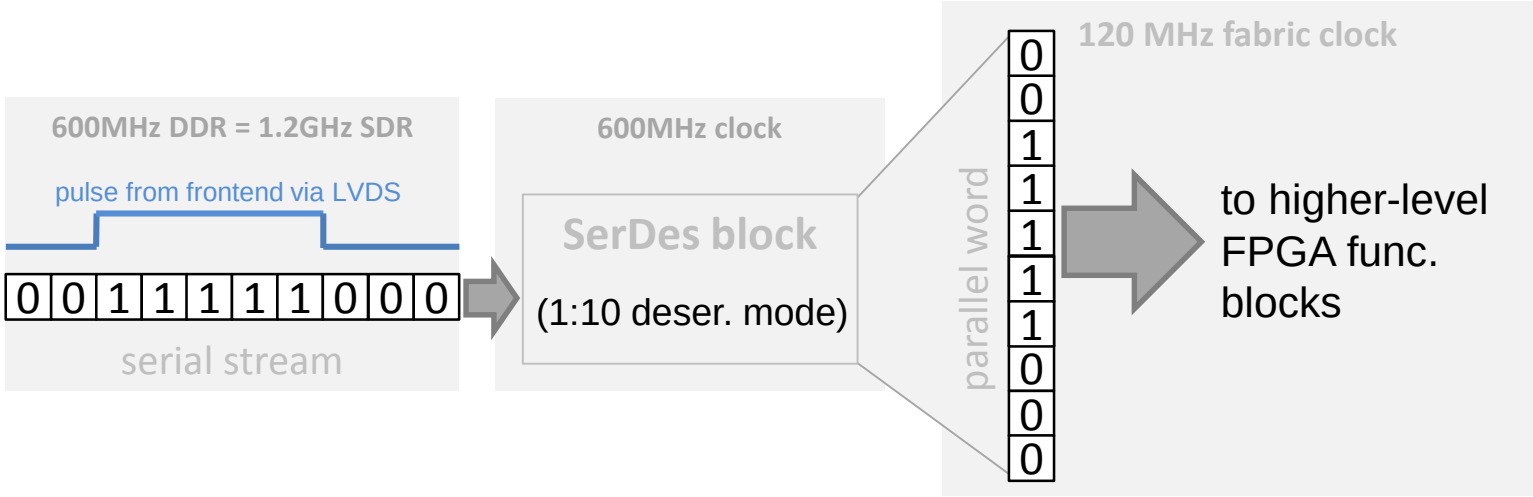
The core component of TDC

The core component of each TDC is a ***SerDes*** Block (same as *ISERDES* by Xilinx)



Deserializers make the highest contribution to the energy consumption of the FPGA

Standard Libero tool provides up to 32 deserialization channels in one hierarchical block. We need however also wider blocks to be generated. These wider blocks are needed for occupying all available pins in a given FPGA bank.

A small spin-off: Python file-generation script for implementing multichannel deserializers was developed. This script can generate Verilog structures (+ VHDL instantiation code) for any number of channels. Restriction: deserializers of only one particular kind (i.e. mode) are available with this script.
Python project: http://github.com/smartfpga/deser_gen