Contribution ID: **38** Type: **not specified**

A Hardware Fast Tracker for the ATLAS trigger

Wednesday, 30 September 2015 10:20 (15 minutes)

The trigger system of the ATLAS experiment is designed to reduce the event rate from the LHC nominal bunch crossing at 40 MHz to about 1 kHz, at the design luminosity of 10^34 cm^-2 s-1. After a successful period of data taking from 2010 to early 2013, the LHC is restarting in 2015 with much higher instantaneous luminosity and this will increase the load on High Level Trigger system, the second stage of the selection based on software algorithms. More sophisticated algorithms will be needed to achieve higher background rejection while maintaining good efficiency for interesting physics signals.
The Fast TracKer is part of the ATLAS trigger upgrade project; it is a hardware processor that will provide, at every level-1 accept (100 kHz) and within 100 microseconds, full tracking information for tracks with momentum as low as 1 GeV/c. Providing fast extensive access to tracking information, with resolution comparable to the offline reconstruction, the Fast Tracker will for example help the High Level Trigger system in the precise detection of the primary and secondary vertices, to ensure robust selections and improve the trigger performance.
The Fast TracKer will exploit hardware technologies with massive parallelism, combining Associative Memory ASICs, FPGAs and high speed communication links.
We present the architecture of the FTK system, the results from integration tests and discuss the expected physics performance in the harsh environment of high pile-up and high luminosities expected for upcoming LHC run-2.

Primary author: ASBAH, Needa (DESY, Hamburg, Germany)

Presenter: ASBAH, Needa (DESY, Hamburg, Germany)

Session Classification: ATLAS DAQ