NEC 2015, Montenegro

A Hardware Fast Tracker for the ATLAS trigger:

The Fast TracKer (FTK) Project

Nedaa Asbah (DESY)
for the ATLAS Collaboration

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nedaa.asbah@desy.de

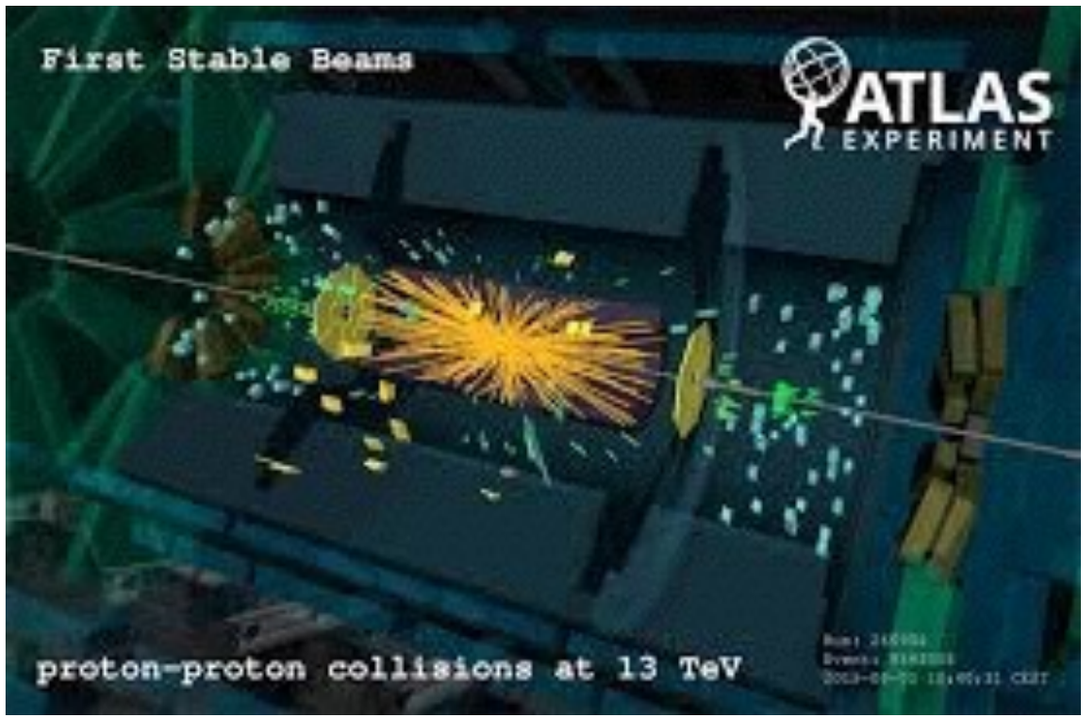
WHY ?

★ **Collisions at 13 TeV started at the LHC**

- Discovering new physics /making precision measurements requires a higher instantaneous luminosity
- RunII will have more than twice luminosity ($1.6x10^{34}cm^{-2}\ s^{-1}$) of RunI ($0.7x10^{34}cm^{-2}\ s^{-1}$)
- Number of interaction per collisions (pile-up, PU)
  - Average of 40-50 (PU) collisions per bunch crossing in RunII
  - It is expected to increase up to 80 (PU) in RunIII

★ **Huge amount of data ~40 Million events per second**

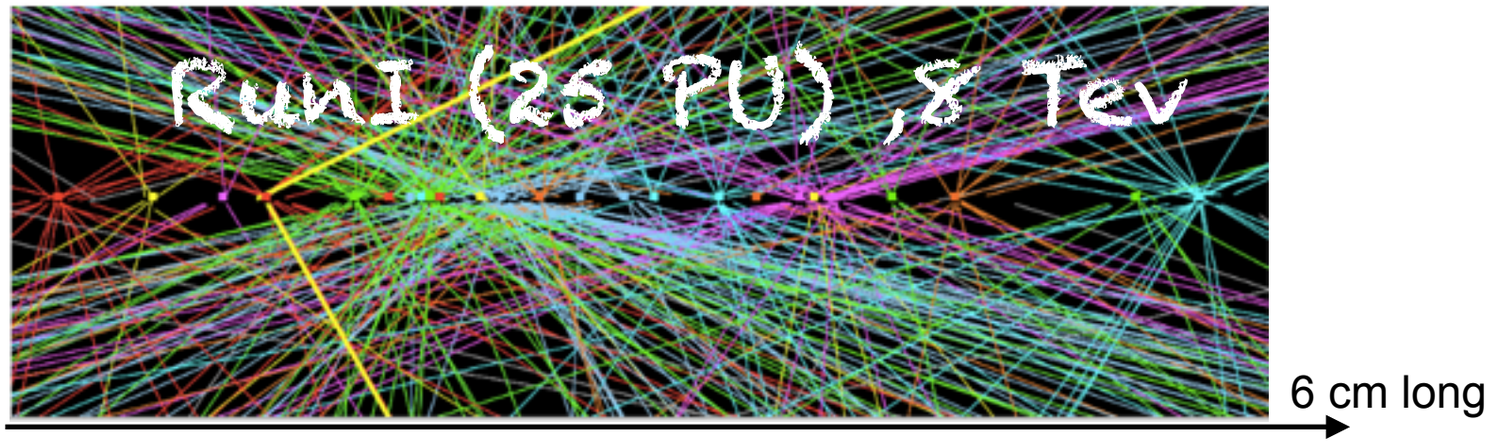
- Need to reduce the data to a manageable rate
- Interesting physics happens rarely
  - Higgs is produced ~1 out of every billion events!
- More sophisticated trigger algorithms become increasingly important combined with high rejection power



WHY ?

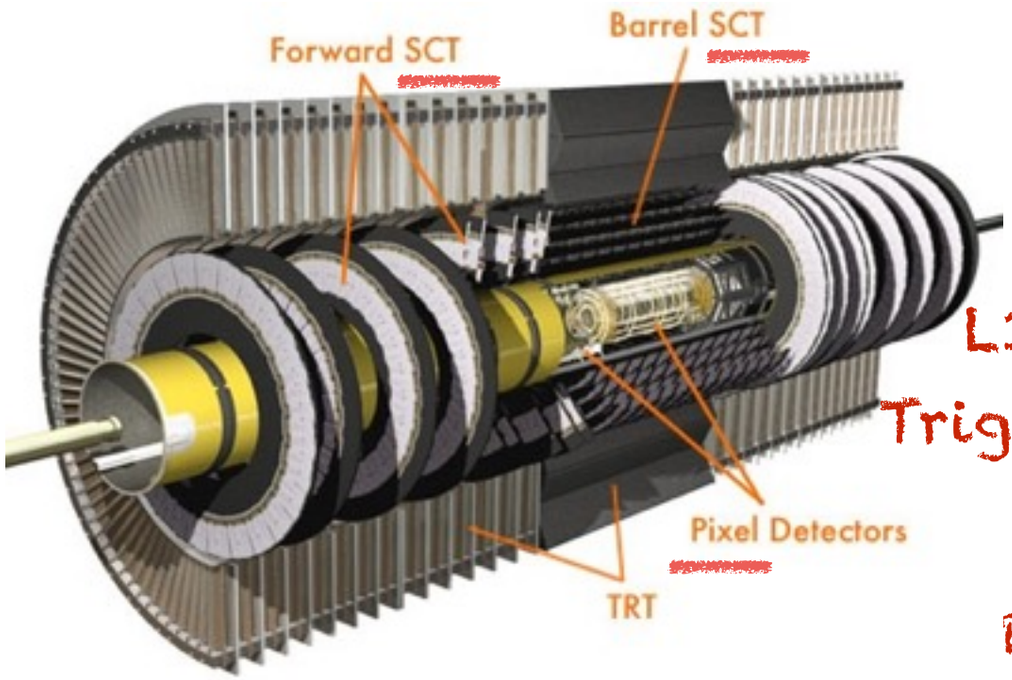
Solution: Fast and precise full event tracking at trigger level to separate the hard scattering and measure its complex details, like secondary vertexes

- measuring number and position of primary vertexes enhance robusteness
- specifically for jet and missing E_T triggers with changing pile-up conditions



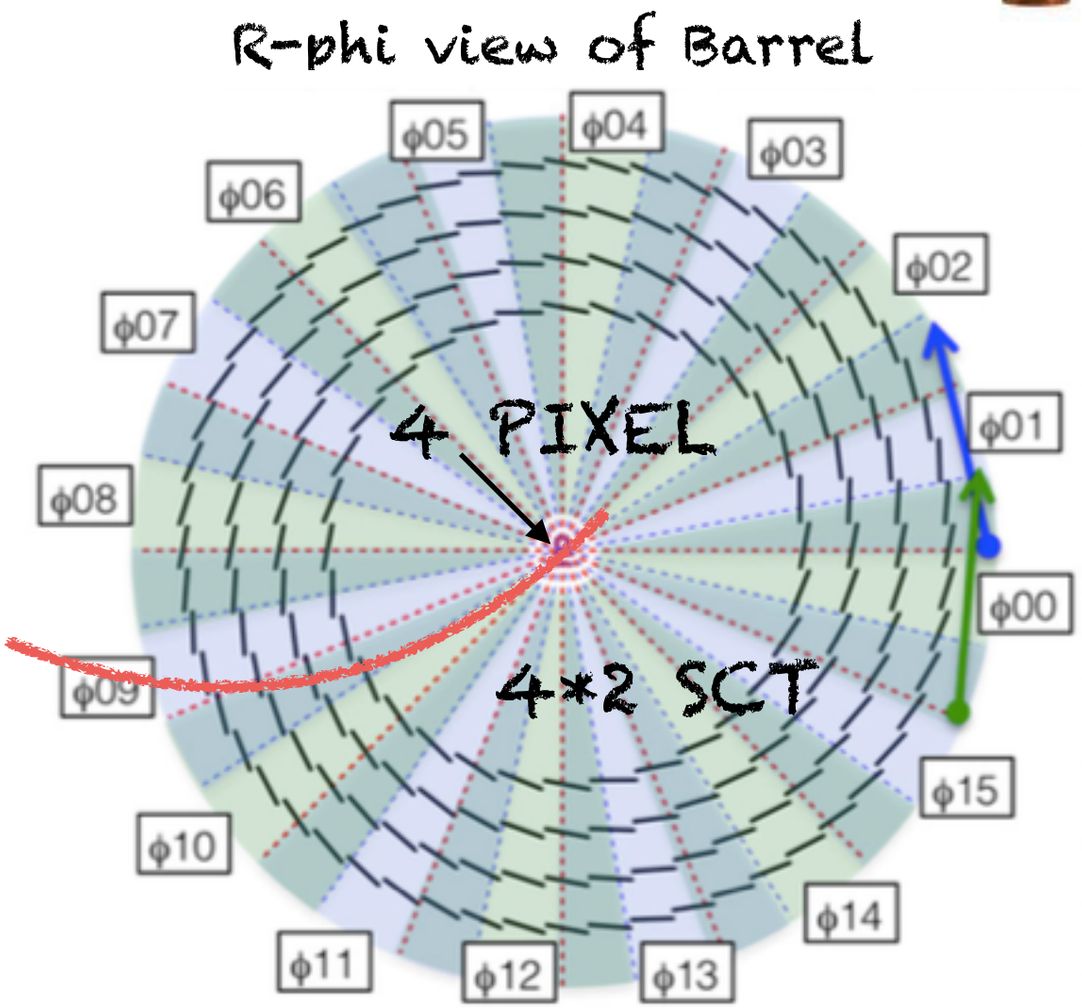
Z → μμ event with 25 reconstructed collision vertices as seen by the inner detector

Fast Tracking in Pixel &SCTDetectors



L1 Trigger

Particles cross 12 detector layers



★ **FTK is very fast (average latency ~100 microsec)**

- ★ Receives and processes data from 98 million channels for every event passing Level-1 trigger (~ 100 kHz)
- ★ Reconstructs charged particles trajectories in the silicon detectors (Pixel & SCT (Silicon Strip Detector)) for p_T > 1GeV and |η| <2.5
- ★ It is made by 128 Processing Units (PUs) working in parallel on the detector divided into 64 towers

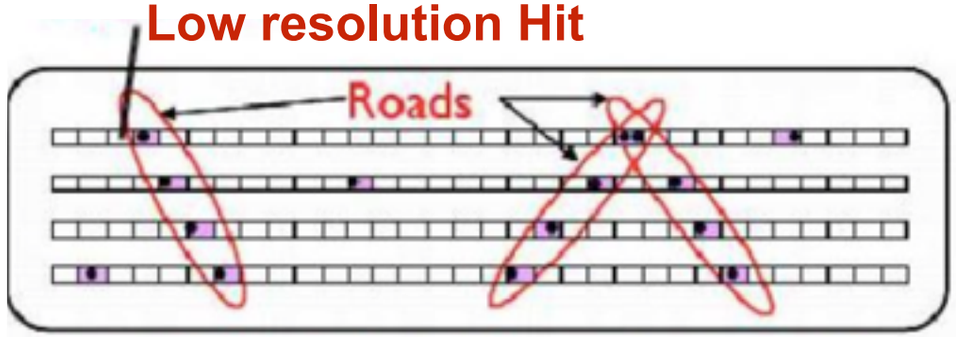
★ **Outputs tracks to be used in High Level Trigger (HLT)**

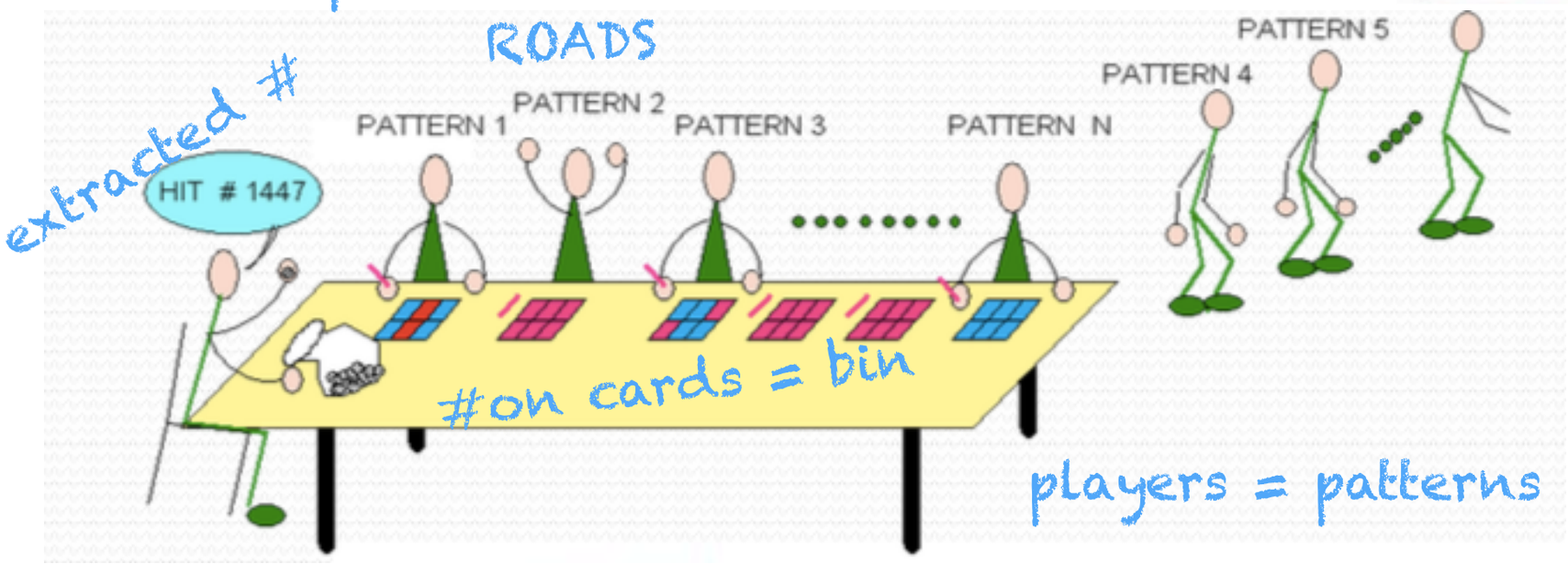
- ★ HLT focuses on algorithms rather than time-consuming tracking!

FTK core Algorithms – Pattern Matching & Track fitting

★ Pattern Matching (PM)

- ★ Carried out by a dedicated highly parallelized hardware, the Associative Memory "AM"
- ★ Possible patterns [low resolution real track candidates] are pre- calculated and stored in Pattern Bank
- ★ Hits in each event are compared with all the patterns in the Pattern Bank and track candidates "ROADS" are found
- ★ Reduce the number of combinations to be sent to the Track Fitting for the few ones contained inside the ROADS



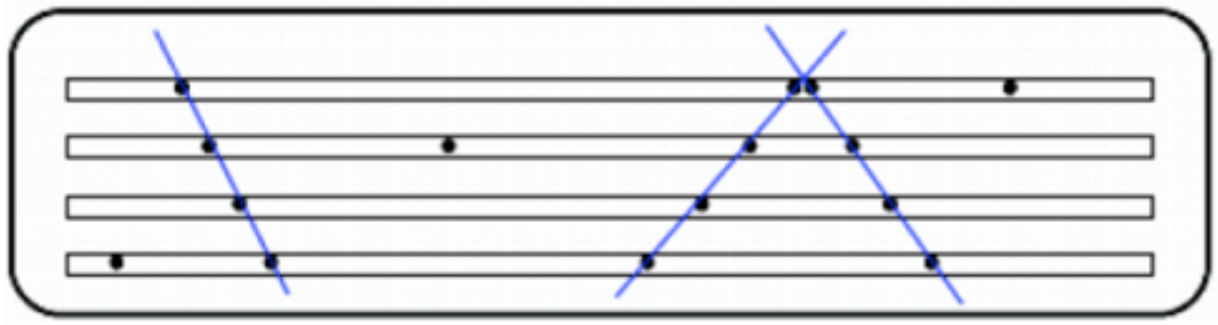


Track Fitting after the Pattern Matching

★ **Track Fitter (TF)**

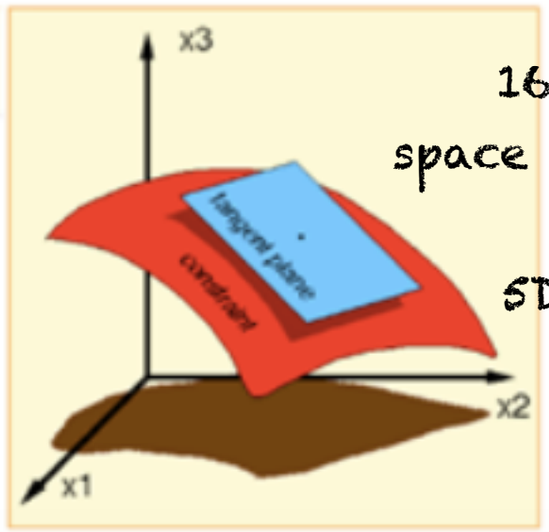
★ Fits the Full- resolution hits inside the road to determine the track parameters

★ The best track is chosen based on the result of χ^2



★ **Track's parameters are evaluated from full resolution hits using a linear Principle Component Analysis algorithm**

ATL-UPGRADE-PROC-2011-004, doi:10.1109/ANIMMA.2011.6172856



16 D coordinates space of hit combinations

5D track surface

helix parameters & χ^2 components

Full resolution hit coordinates in the Silicon layers

$$p_i = \sum_{j=1}^{16} a_{ij} x_j + b_i$$

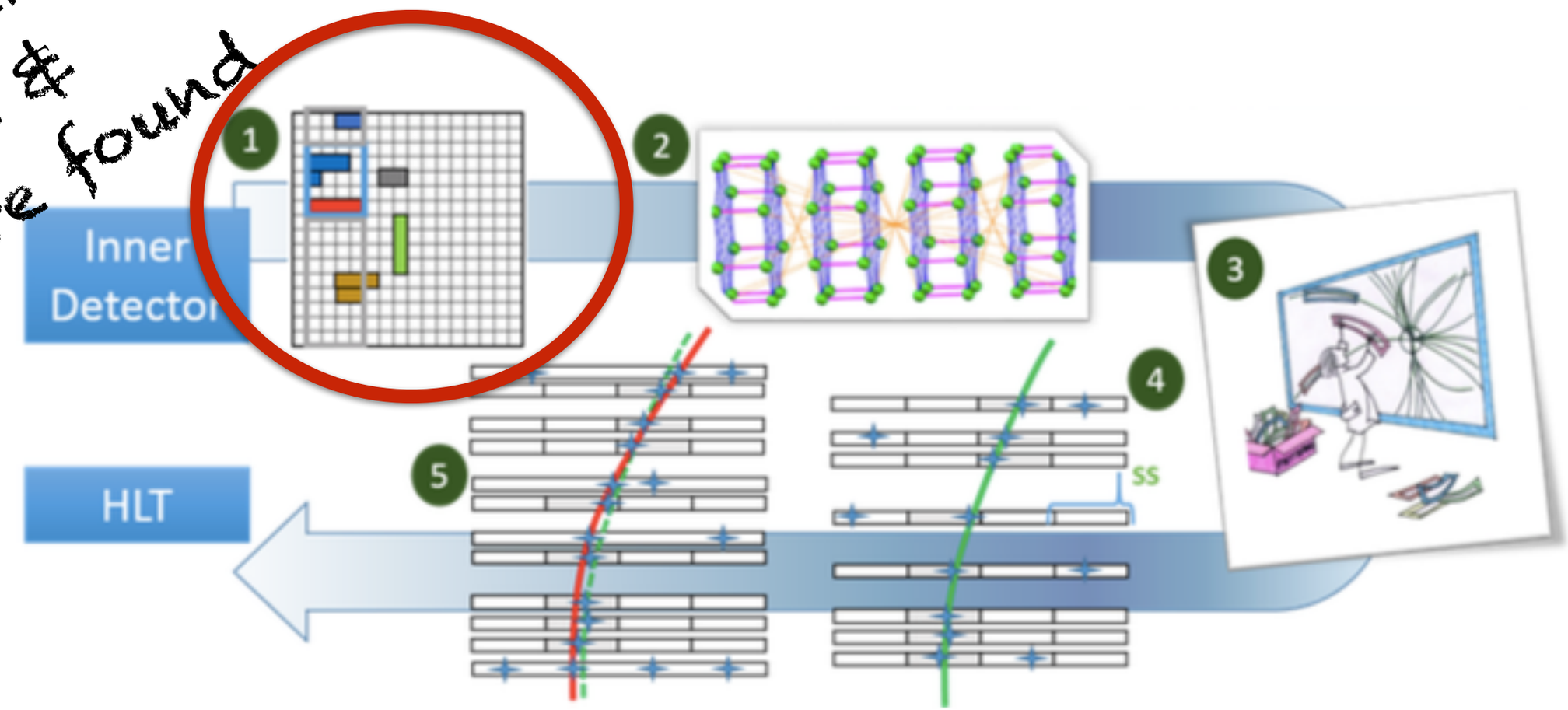
pre- stored constants determined from full simulation or real data tracks

★ **TF is very fast; each FPGA (Xilinx Kintex 7 Series, ARRia 5,…) outputs one fit results each ns!**

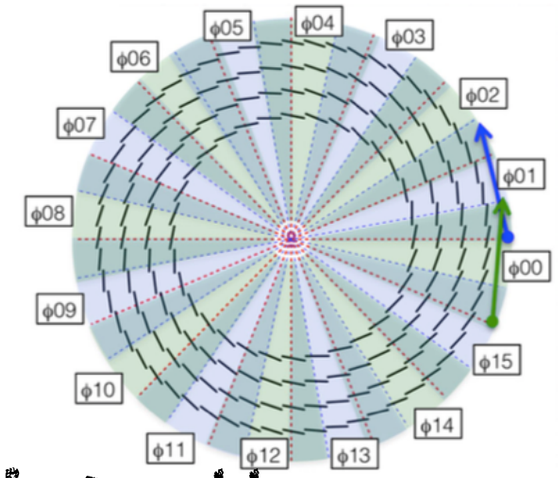
Data Flow: Best estimate of the particle position on the silicon

Custom pixel clustering and centre of gravity calculation for each cluster on FPGAs

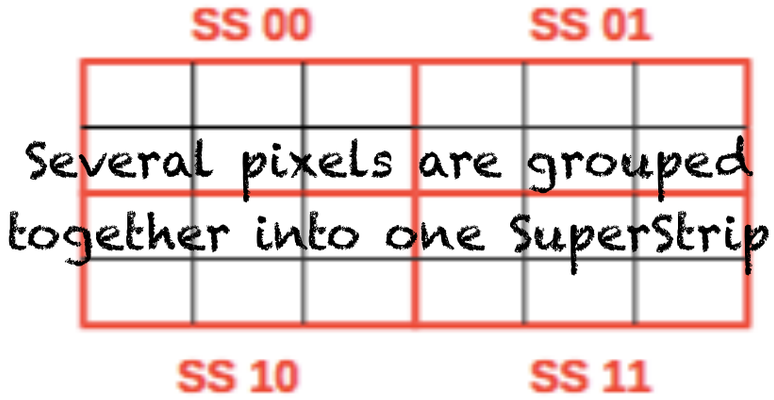
Raw data are received & clusters are found



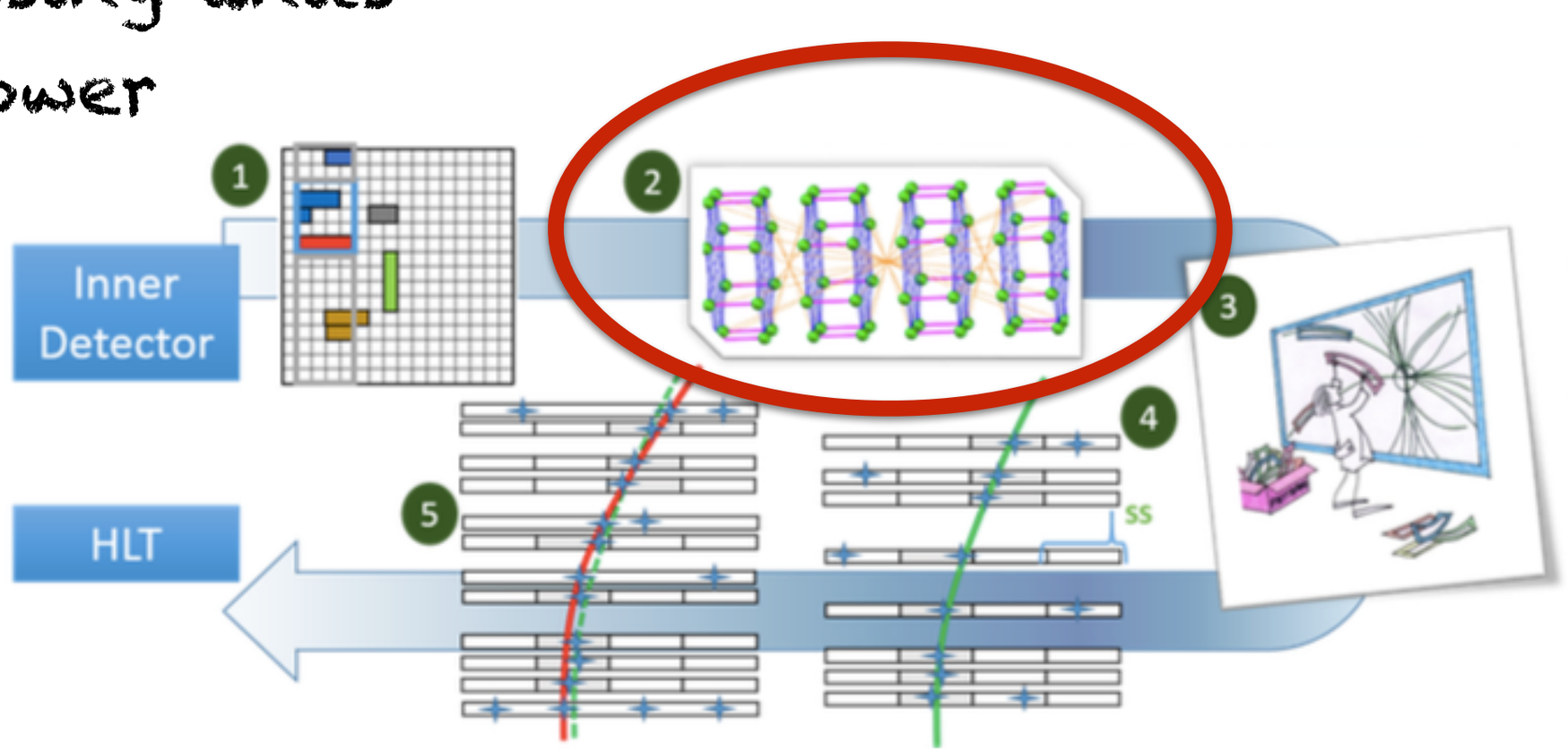
Data Flow: Data distribution to the 64 towers



Geometrically grouped data distributed to two processing units per tower

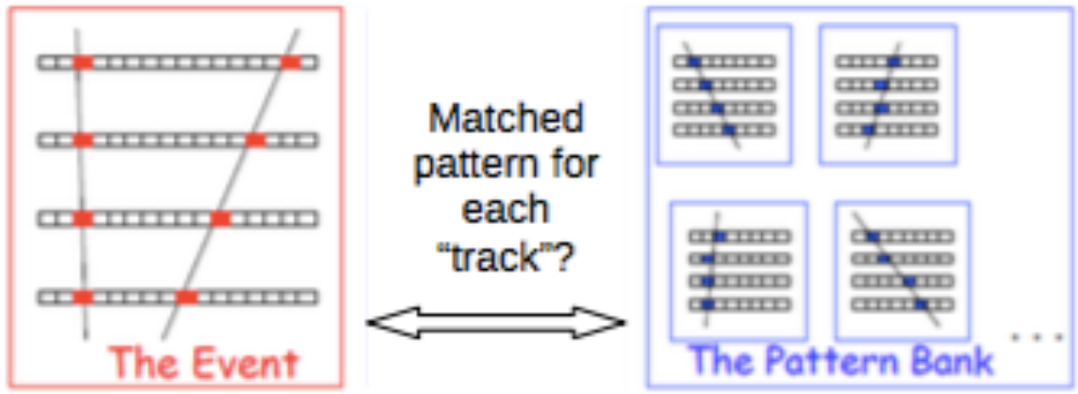


Transformation to coarse- resolution hits

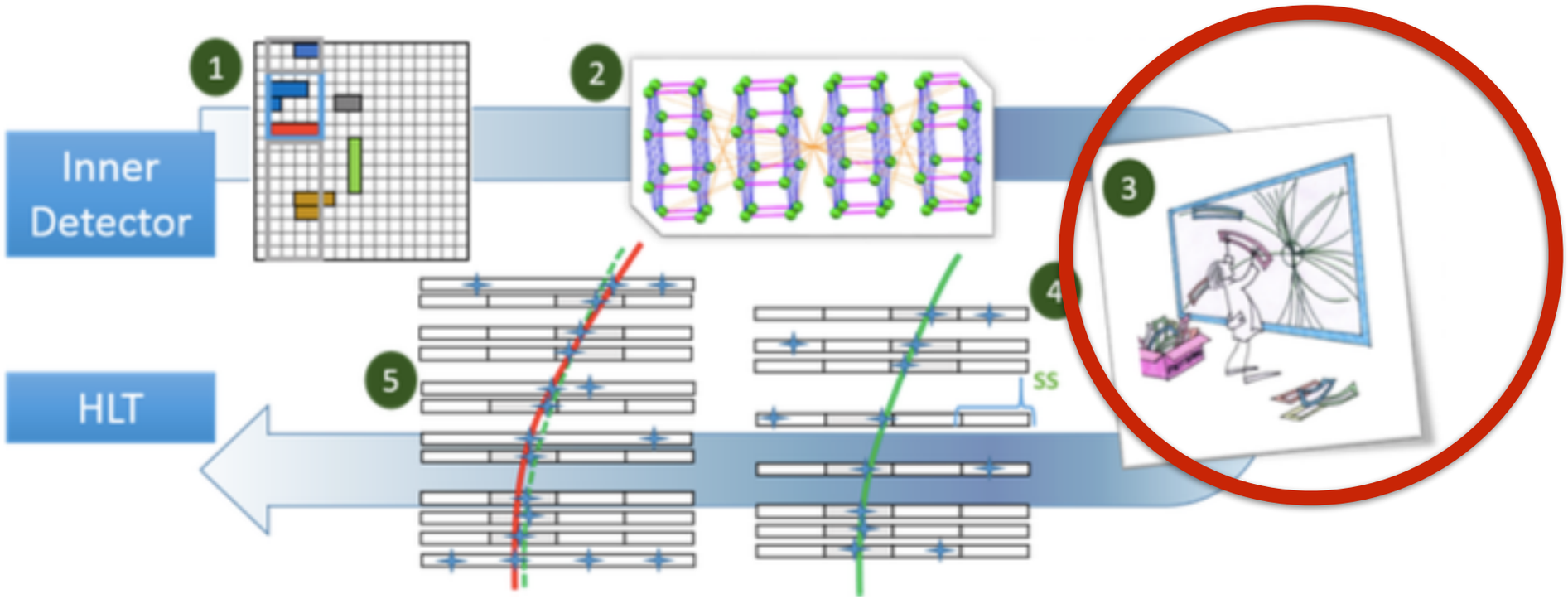


Data Flow: Pattern matching to find roads

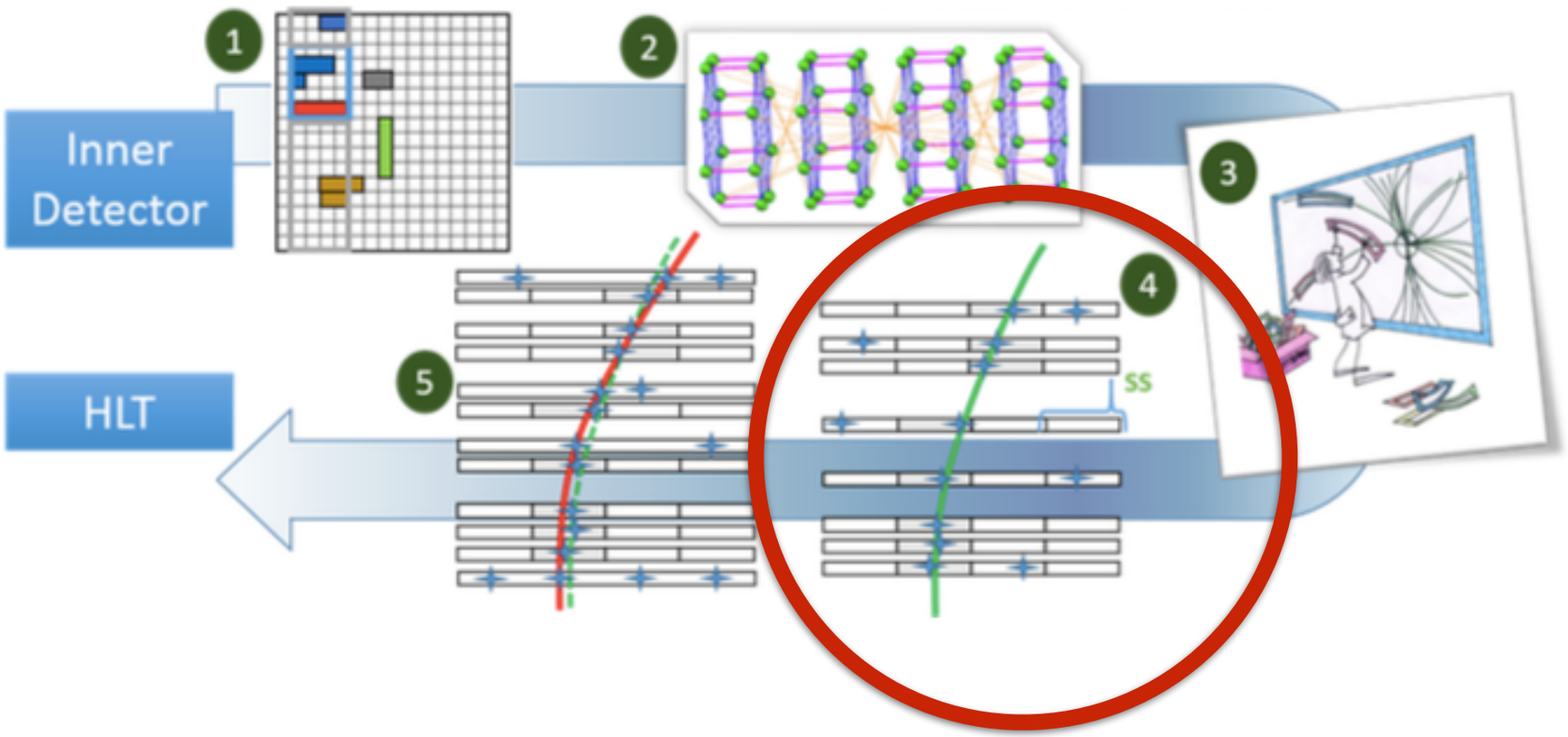
Event data compared to patterns at coarse resolution



Stored in associative memory



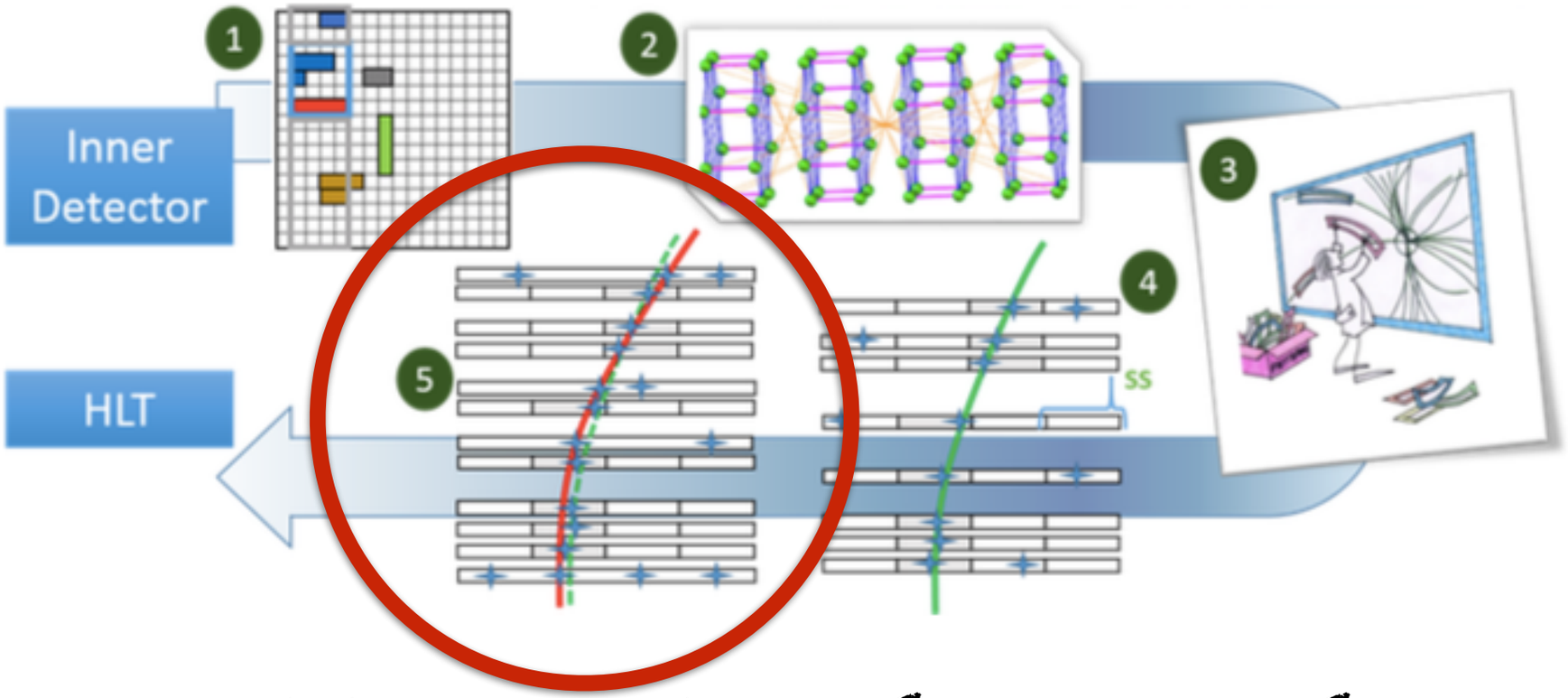
Data Flow: First Track fitting step inside roads



First track fit is performed with 8 layers only

Reduce the hit combinatorics inside the roads to be sent to next fit stage

Data Flow: Second track fitting step & adding 4 extra layers

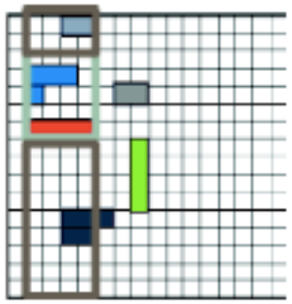


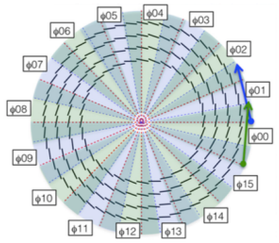
Use in addition, data from the four layers not included in the previous stage fit.

*To reduce the fake tracks; higher layer information is needed to chose the best track

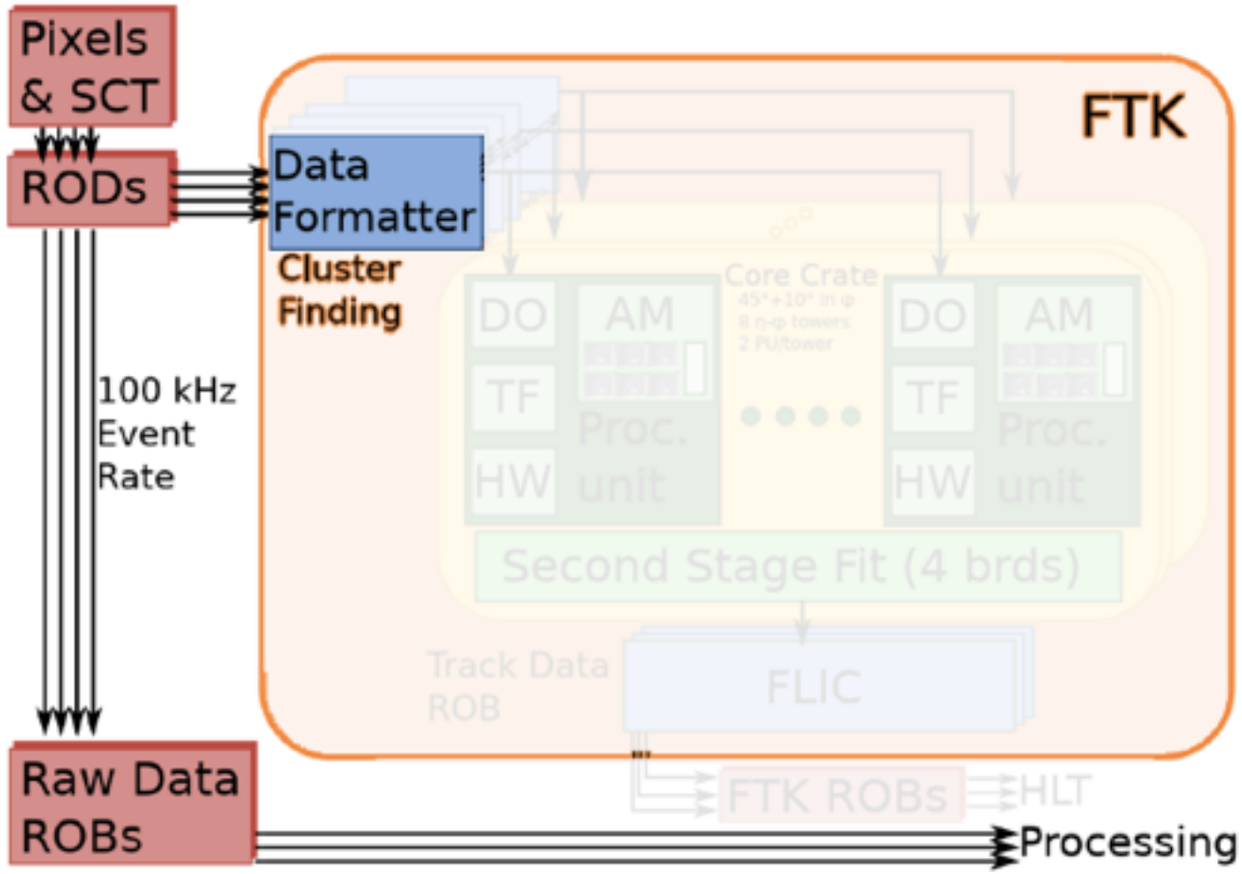
*Improve the parameter's resolutions

FTK Hardware components





32x Data Formatter (DF) & each DF has 4 Input Mezzanines (IM)

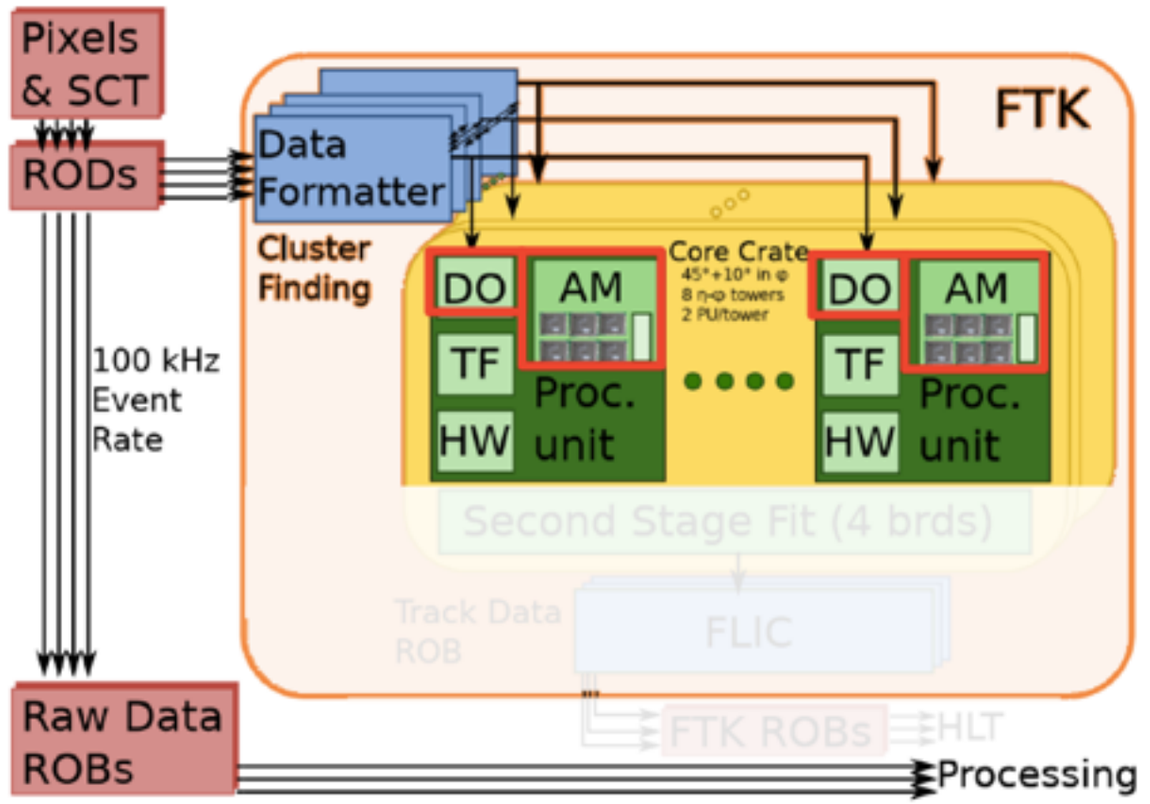


- ★ **Dual-output high-speed optical link (SFP using S-Link protocol- CERN) splits SCT/Pixel data for DAQ and FTK**
- ★ **128 IM receive 4 Slink for a total data traffic of 500 Gbps between the detector front end and FTK**
  - ★ **Receive the SCT/Pixel hits and clusters them**
- ★ **DF sorts the hits into their FTK η/φ towers and delivers them to processing units (PU)**

FTK - Hardware components

128x Auxiliary Boards (AUX)

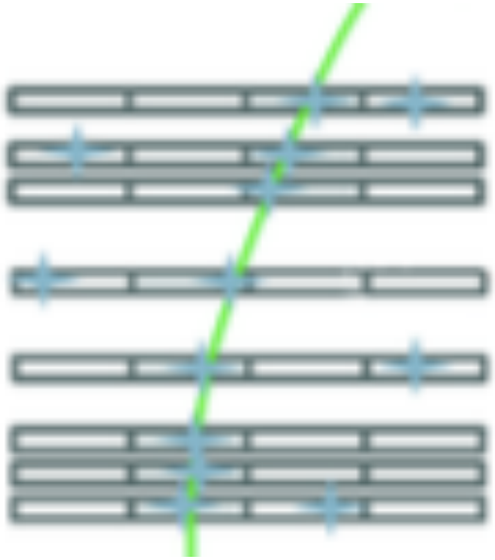
& 128x Associative Memory Boards (AMB)

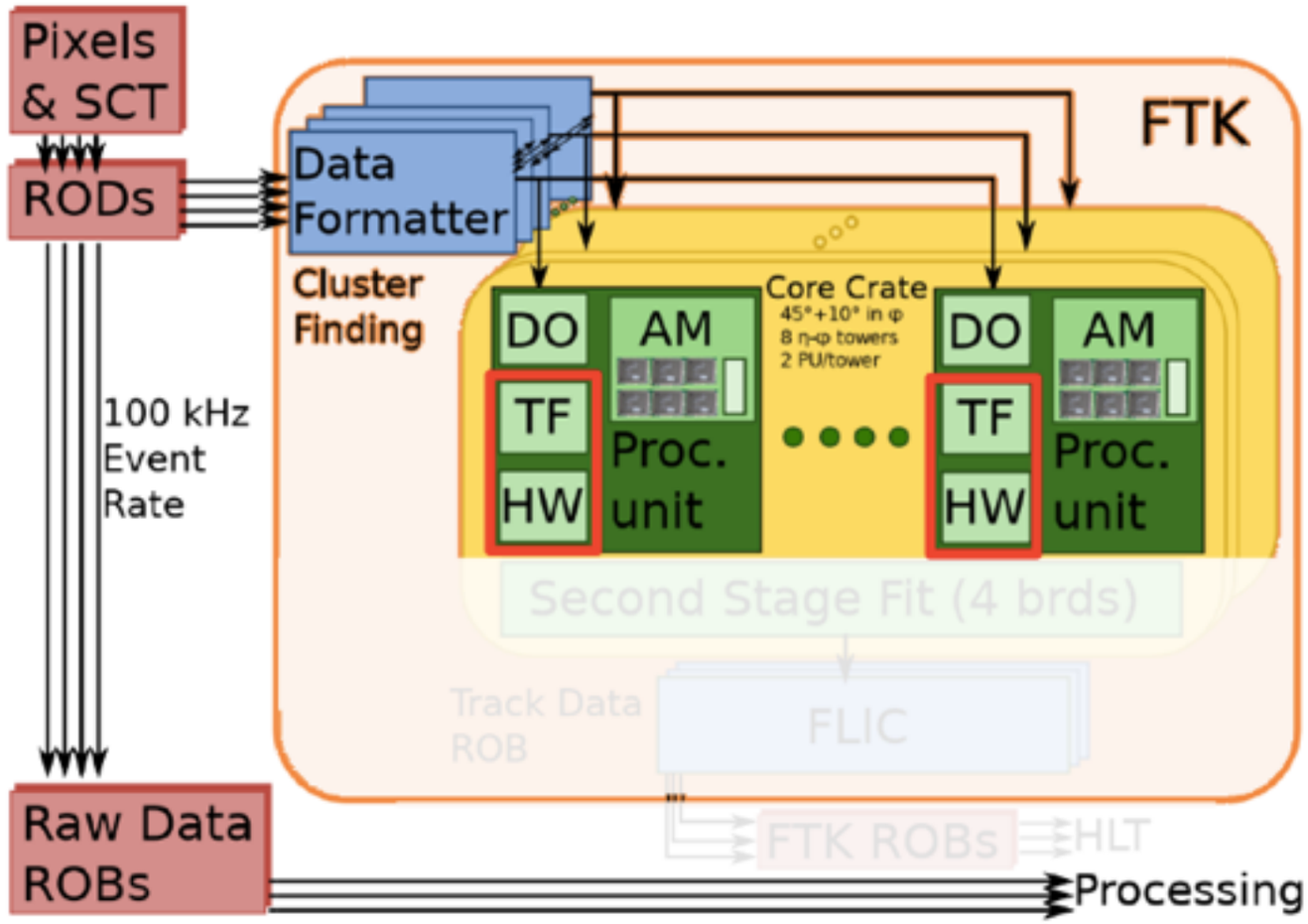


- The processing units consist of the Auxiliary (AUX) Card and Associative Memory Board (AMB)
- AUX receives hits from a DF on 2 QSFP+ fibre blocks.
- AUX sends full resolution hits to Data Organiser (DO) for storage & makes coarse resolution hits to send to AM
- AMB contains 64 AMchips divided into 4 mezzanine, 16 chip per mezzanine
- AM finds the possible tracks the hits can belong to
  - the challenge here is to manage the size of the stored bank

FTK - Hardware components

First Stage Fit



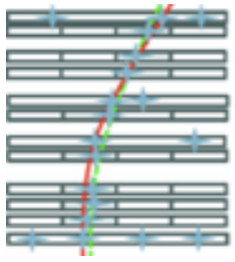


★ **AUX Track Fitter (TF) takes full resolution hits from DO after matching and does χ^2 fit on track parameters, outputs tracks passing χ^2 cut**

★ **AUX Hit Warrior (HW) removes duplicate tracks**

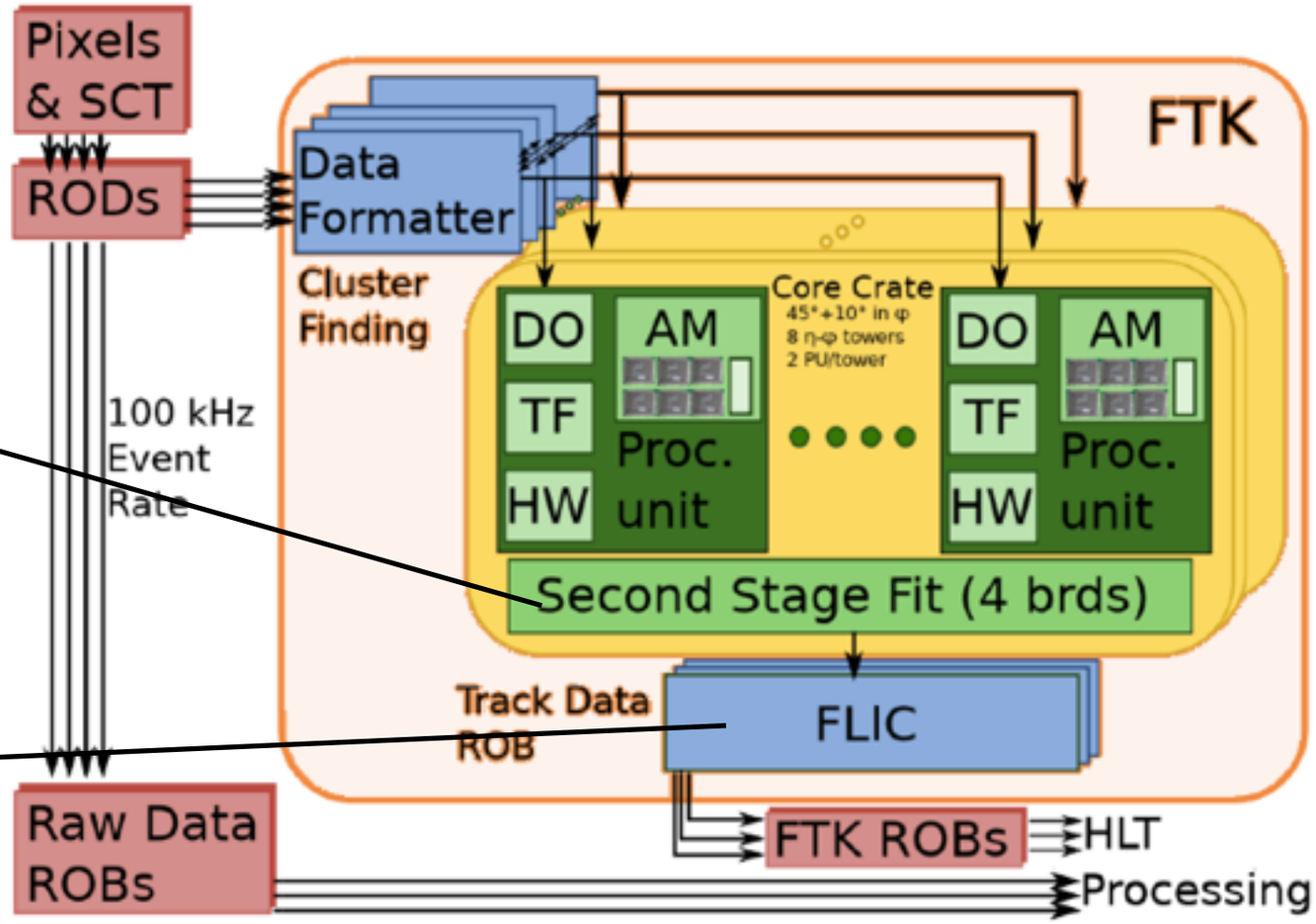
★ **Main processing units are high-performance Altera FPGAs (Arria V)**

FTK - Hardware components



32x Second Stage Board (SSB)

2x Level-2 Interface Crate (FLIC)



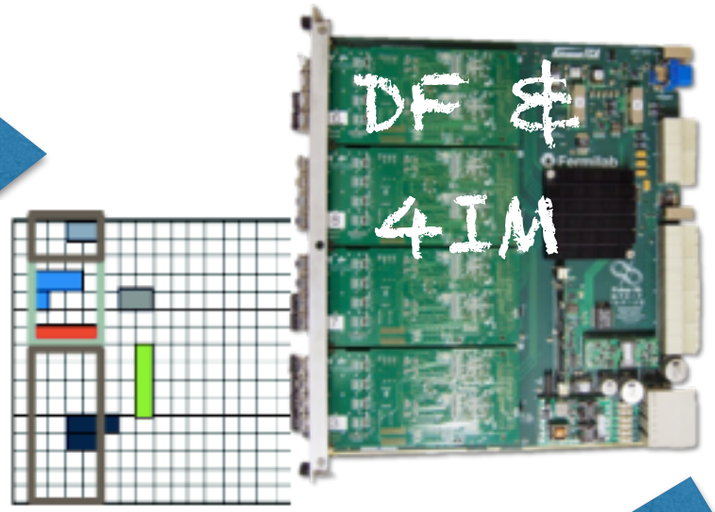
★Second step of the fit is done by the SSB

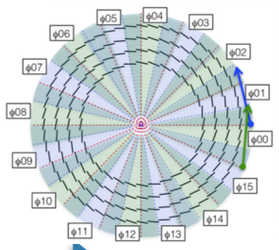
★A Rear transition module (SSB RTM) receives the data from the DF
★ Contains a series of QSFP & SFP+ modules with signals routed to a high-speed connector in the P3 area
★All tested at 6.4 Gbps

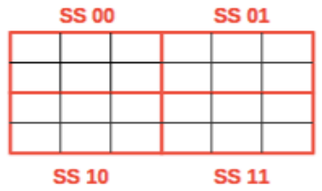
★ FLIC reformats the track records into the standard ATLAS event format and sends them to High Level Trigger Read Out Systems

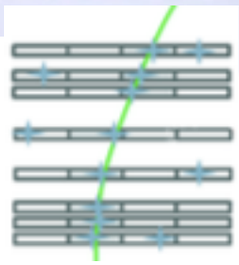
Data Flow - Hardware

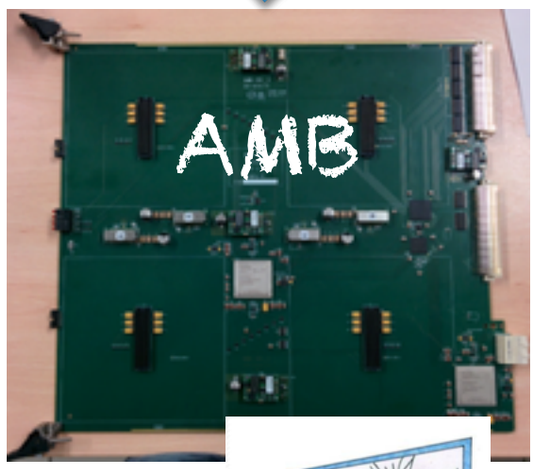
Pixel & SCT

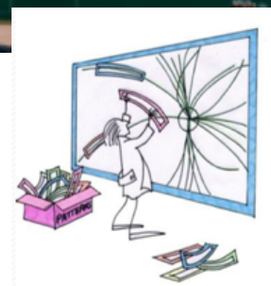


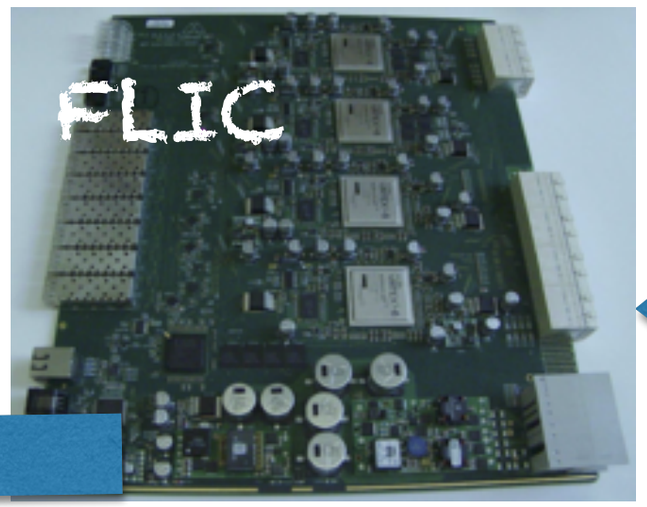




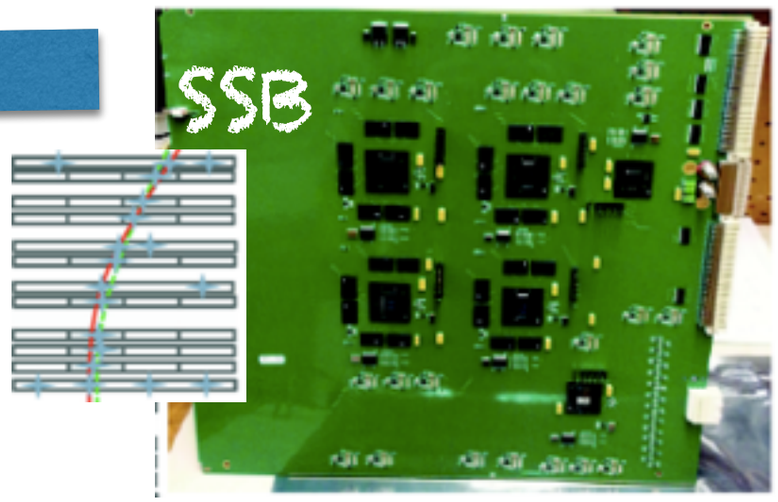




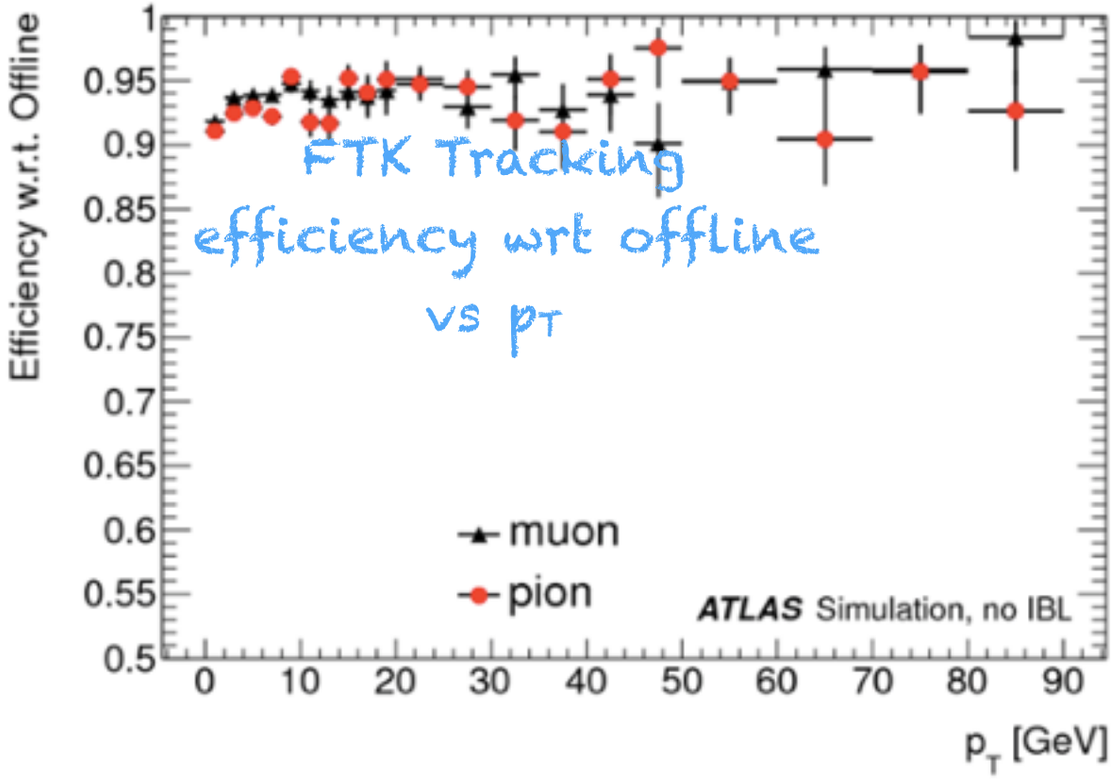


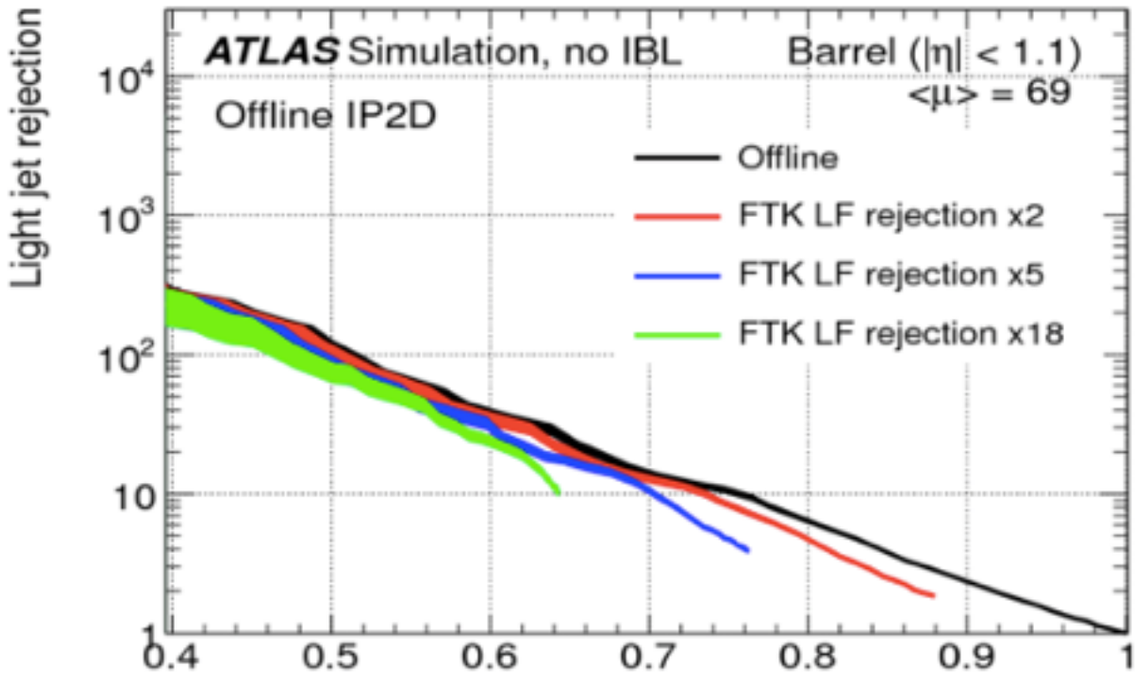


HLT



Expected FTK performance





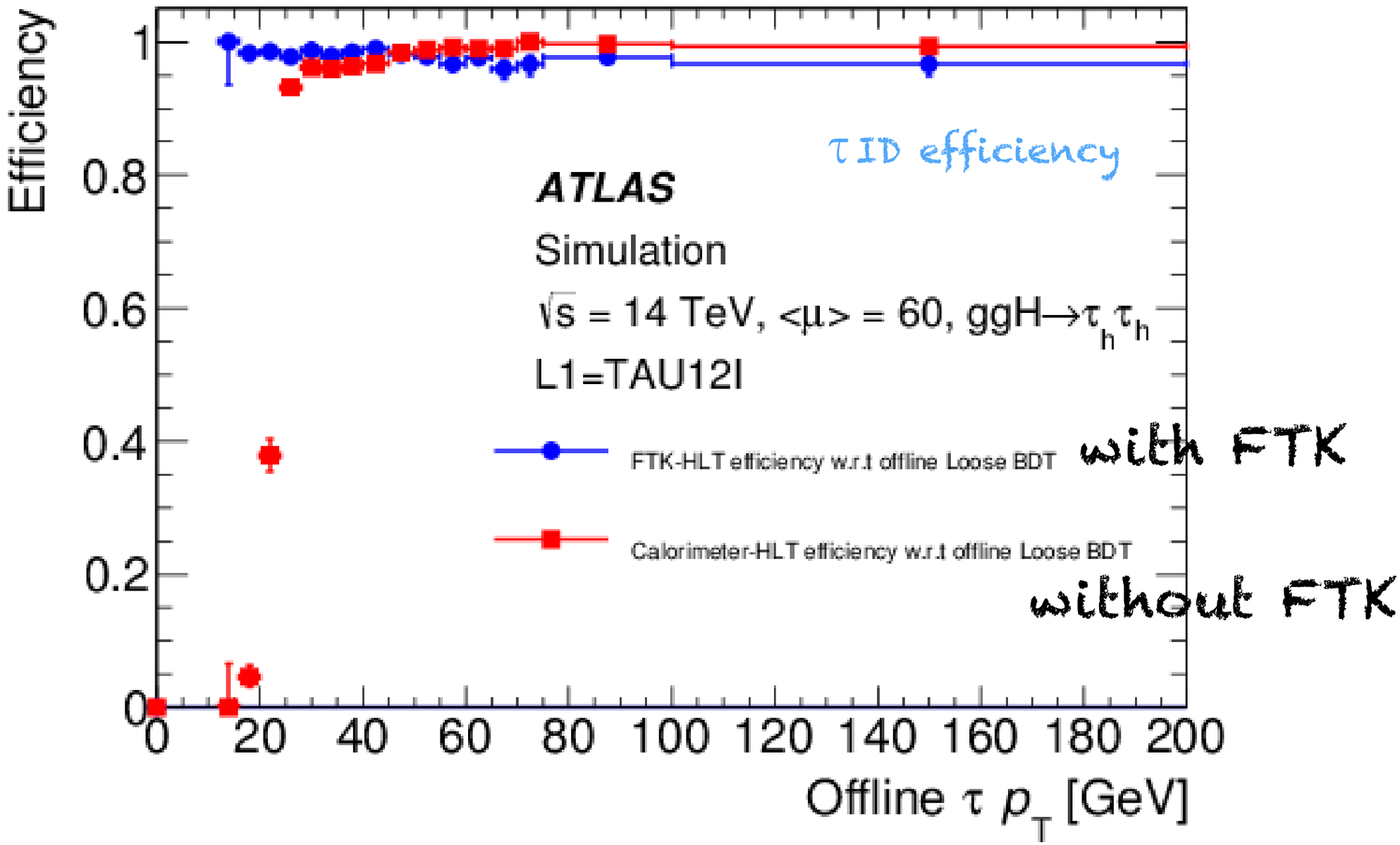
B- Tagging using FTK tracks after refitting

- **FTK tracks generally have a resolution comparable to the offline algorithms**
  - Efficiency of 95% with respect to the offline tracking (as function of muons, pions p_T)
  - Fake rate of 5% at pileup 70
- **Similar b-tagging efficiency with high online light-jet rejection**

Expected FTK performance

- **Number of FTK found vertexes is proportional to the number of vertexes found by offline independently of the amount of pileup**

- **Trigger efficiency for τ in H->$\tau\tau$ significantly improved at low p_T**
  - Using optimised algorithms with FTK tracks



Summary

- FTK will be able to provide high quality tracks to HLT for all L1 accepted events
  - High speed using FPGAs and ASIC devices built on purpose, the Associative Memories
- Allows HLT to collect a wider range of interesting physics channels
- Using tracking information to better identify taus and b-jets
- FTK will help in reducing sensitivity to pileup
- Precise reconstruction of the collision vertices
- FTK track quality and efficiency compatible with the offline performance
- Most of the hardware is ready for production
- First complete slice of the system will be ready for testing during 2016 ATLAS data taking
  - Barrel region coverage as of spring 2016
  - Full coverage towards the end of 2016

We have a very interesting time ahead of us at the LHC

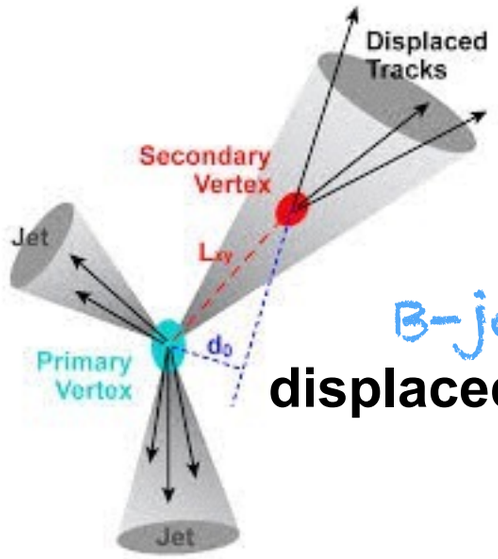
Thank you!

BACKUP

WHY ?

★ Higgs Found! SM-like ??

- ✦ Fermionic- coupling measurements are essential to understand Higgs properties
- ✦ Channels with b and τ final states are very important but they suffer from
  - ✦ Large QCD backgrounds
  - ✦ Low trigger efficiency

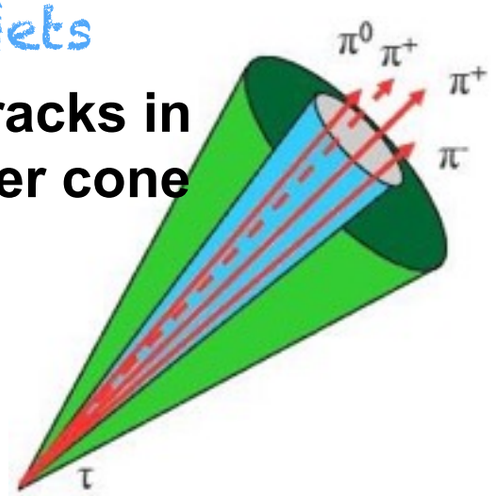


B-jets

displaced vertex

τ-jets

fewer tracks in a smaller cone

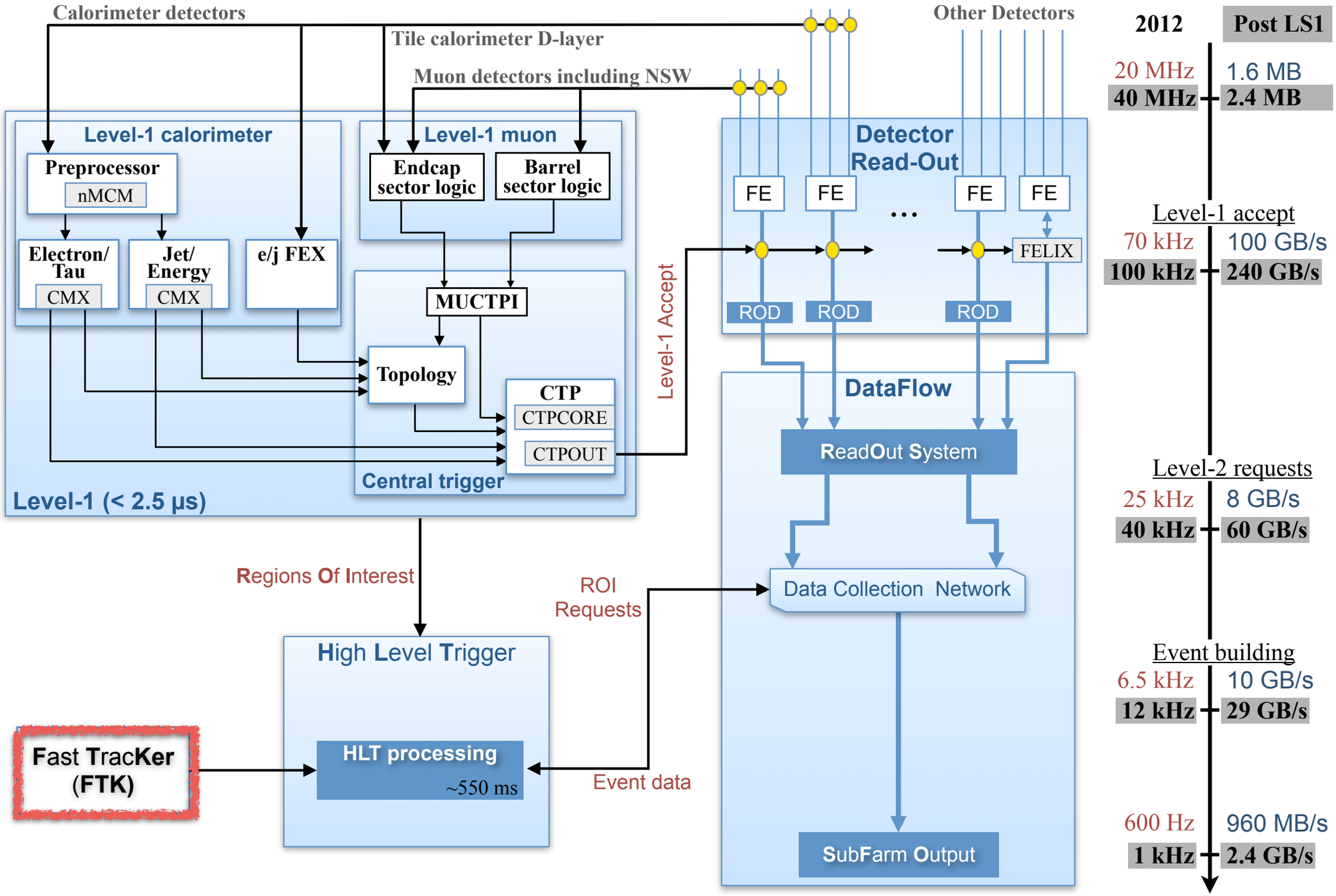


★ SUSY could be hiding!!

- ★ final states of b's and τ's (difficult to select and trigger)

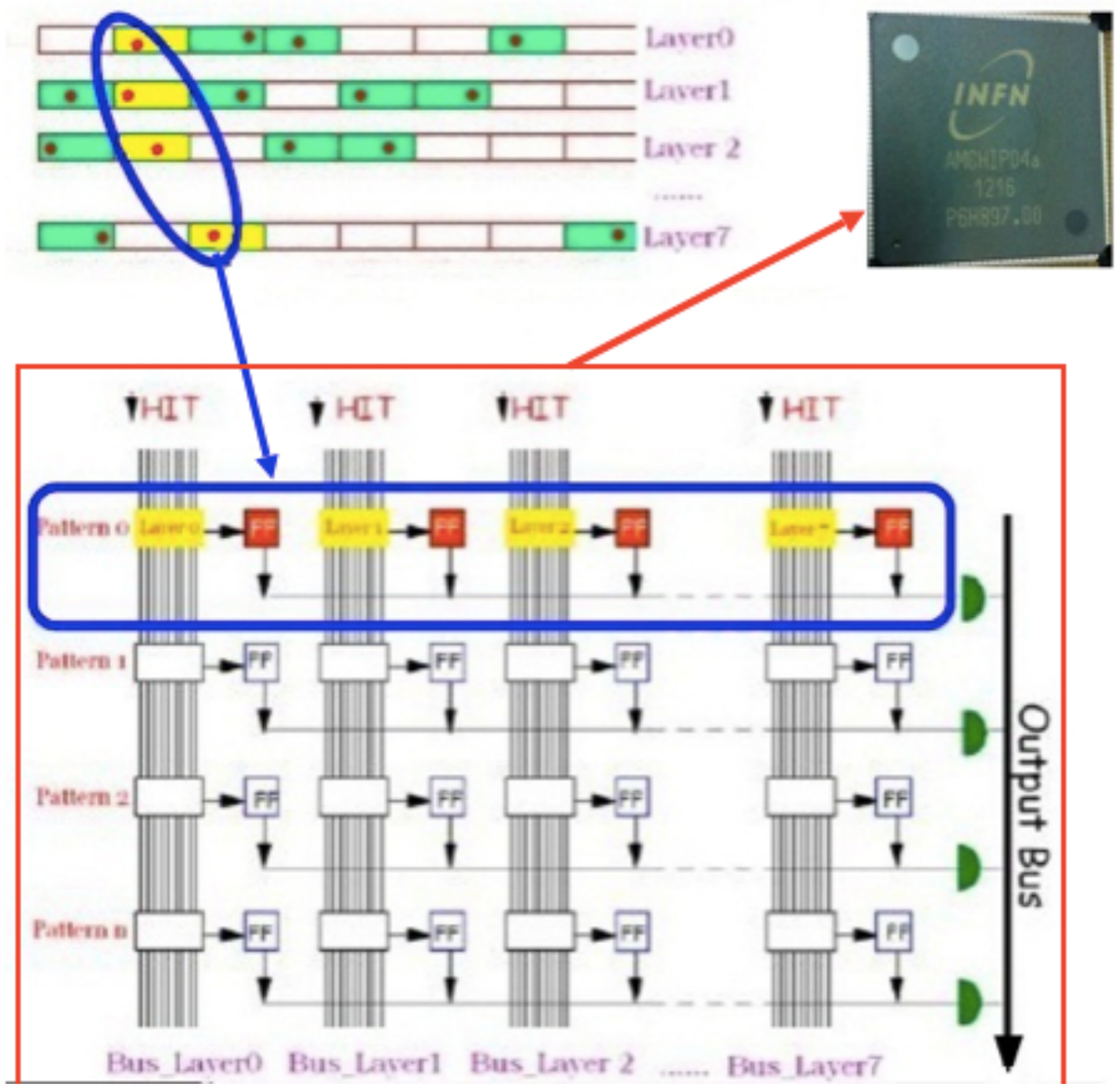
→ **Better tracking of b and τ jets are trigger level is important for such analyses**

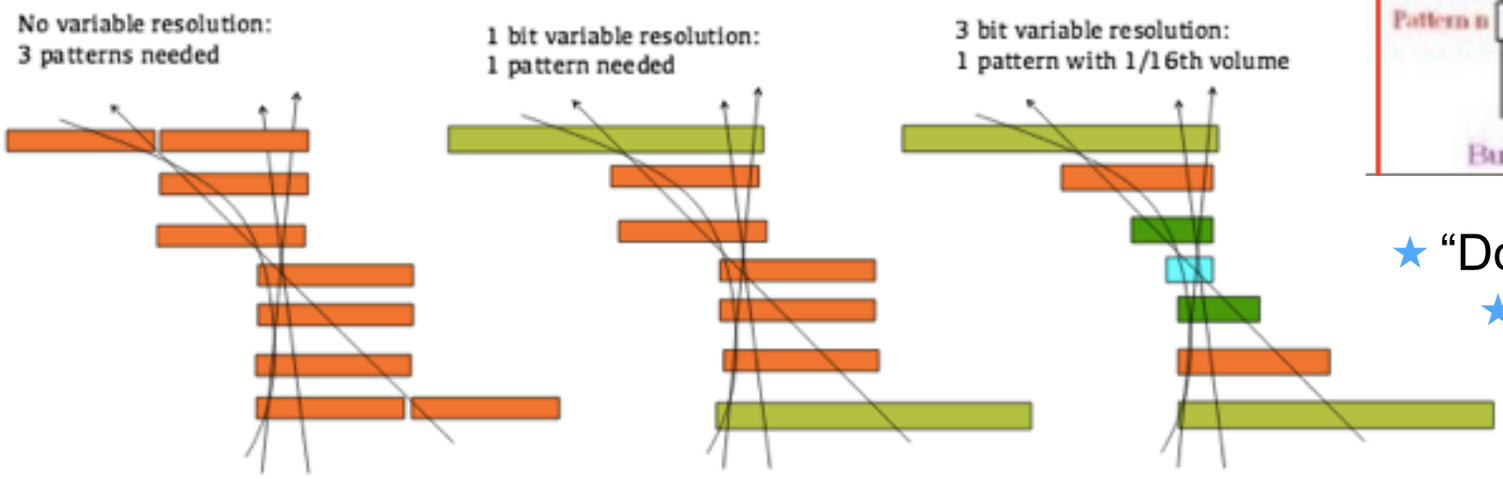
ATLAS Trigger System



Associative Memory Board

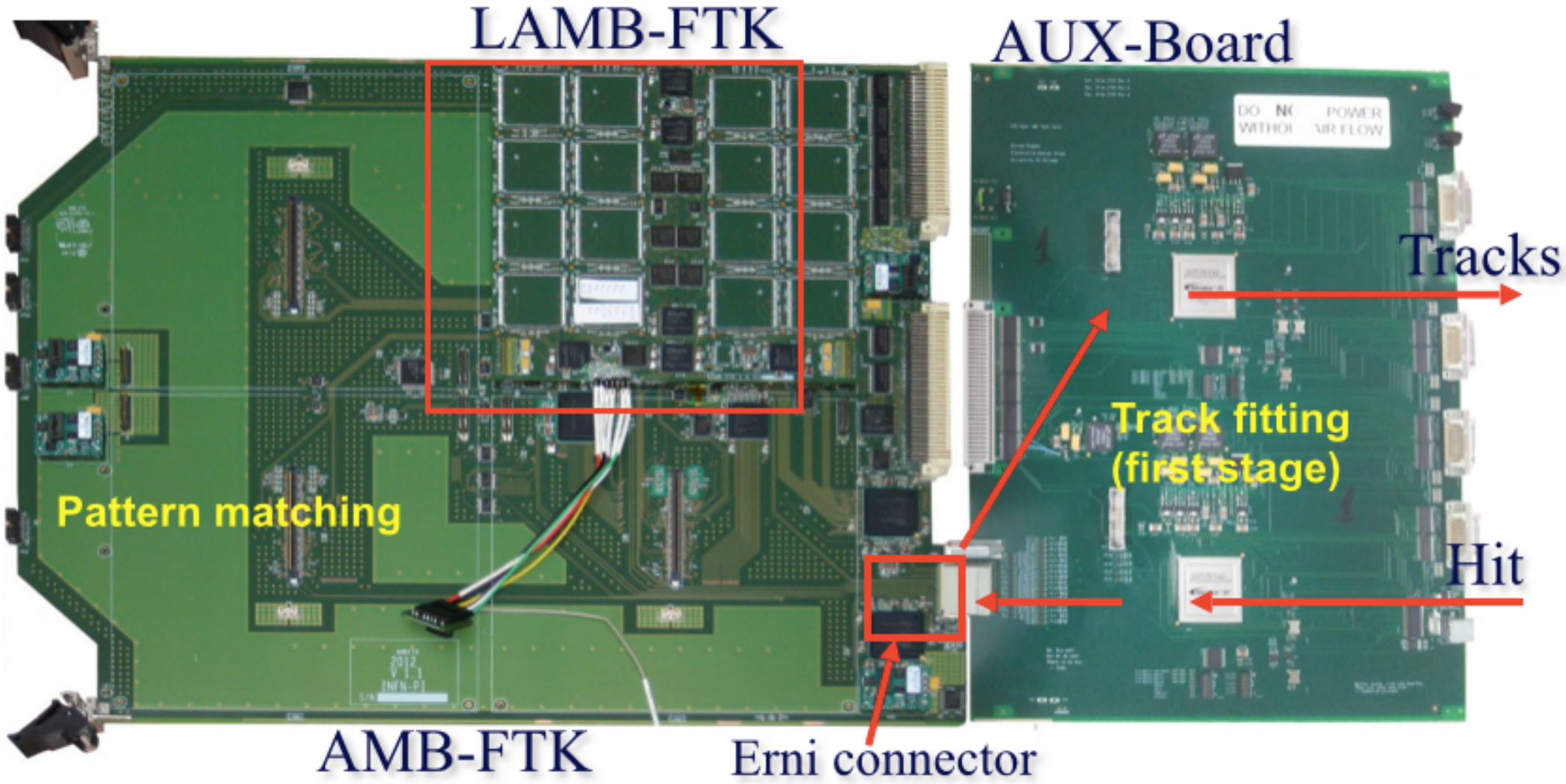
- ★ AM chip is a special CAM chip
- ★ Identifies the presence of stored patterns in the incoming data
  - ★ Data arrives through 8 independent busses
- ★ Consumption:
  - ★ ~2.5 W for 128 k patterns
  - ★ Performing 10^{14} parallel comparisons at 16 bits per second



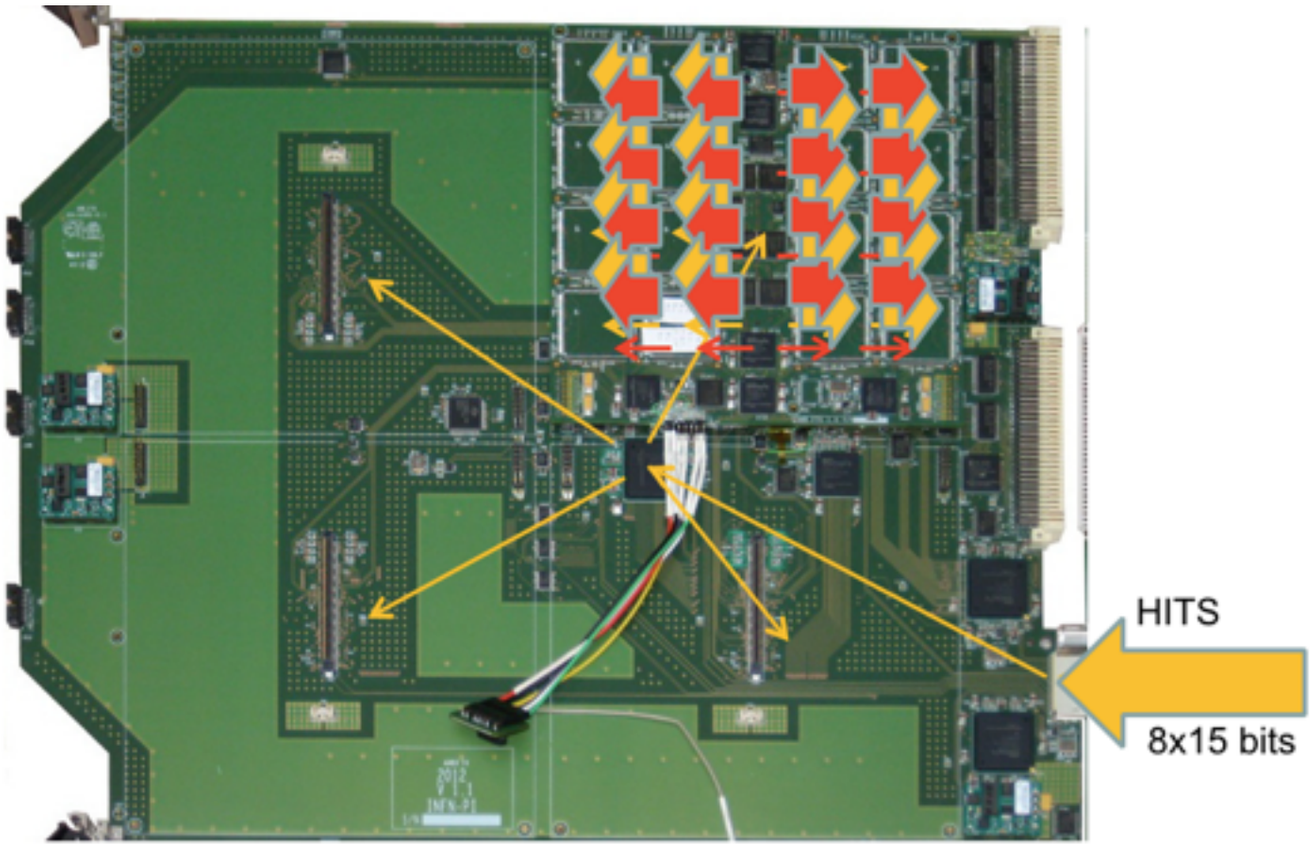


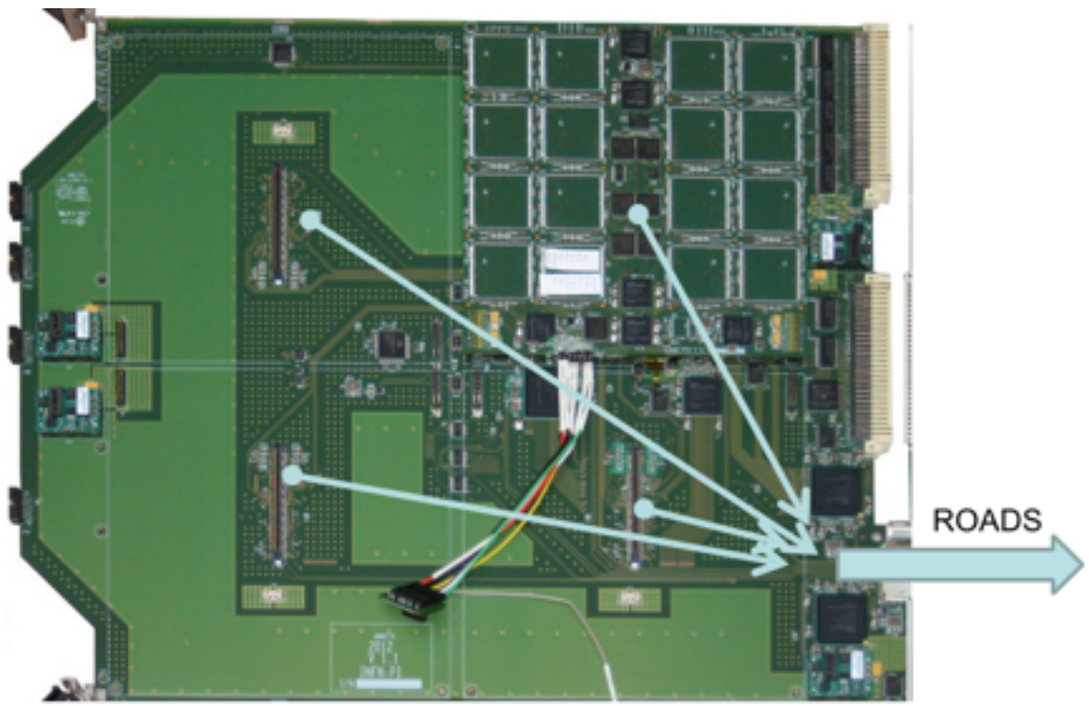
- ★ "Don't Care Bits"
  - ★ Reduce the number of patterns and fake matches

AM - processing unit



AM - DataFlow

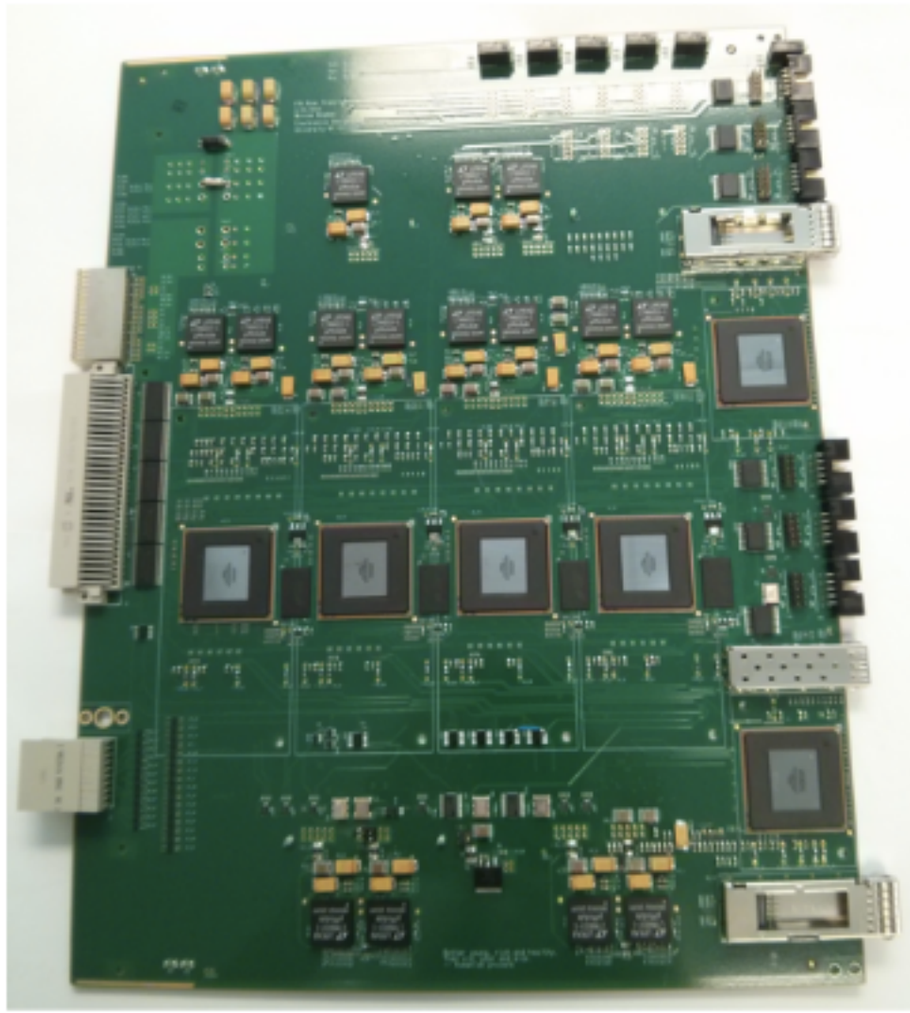


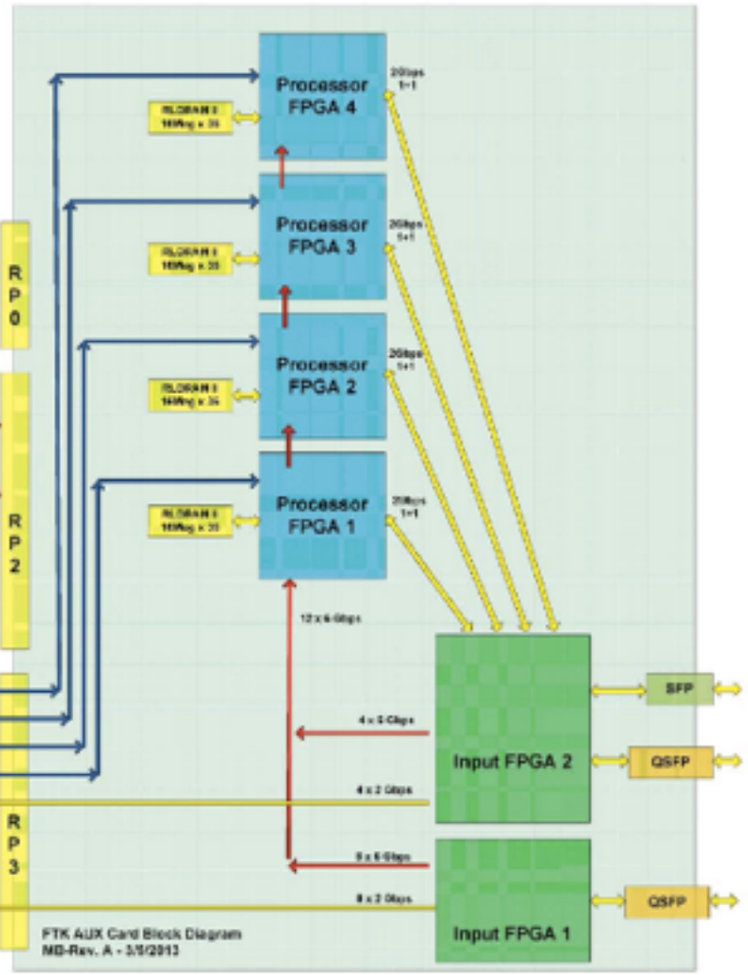


128 AM boards
are needed

AUX

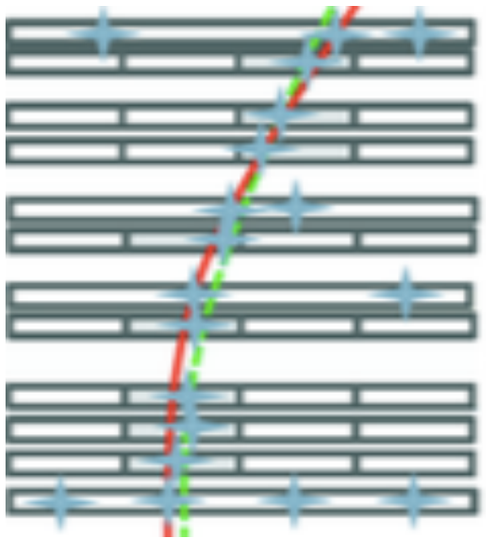
- ★ AM board had multifunctional Auxiliary Card
  - ★ VME Control though main board through P2 connector
- ★ Convert clusters to Super Strips “SS”
- ★ Receives matched road IDs and fetches full resolution hits
- ★ Performs 8 layer fit to reject bad roads
- ★ Sends roads to SSB for 12 layer fit

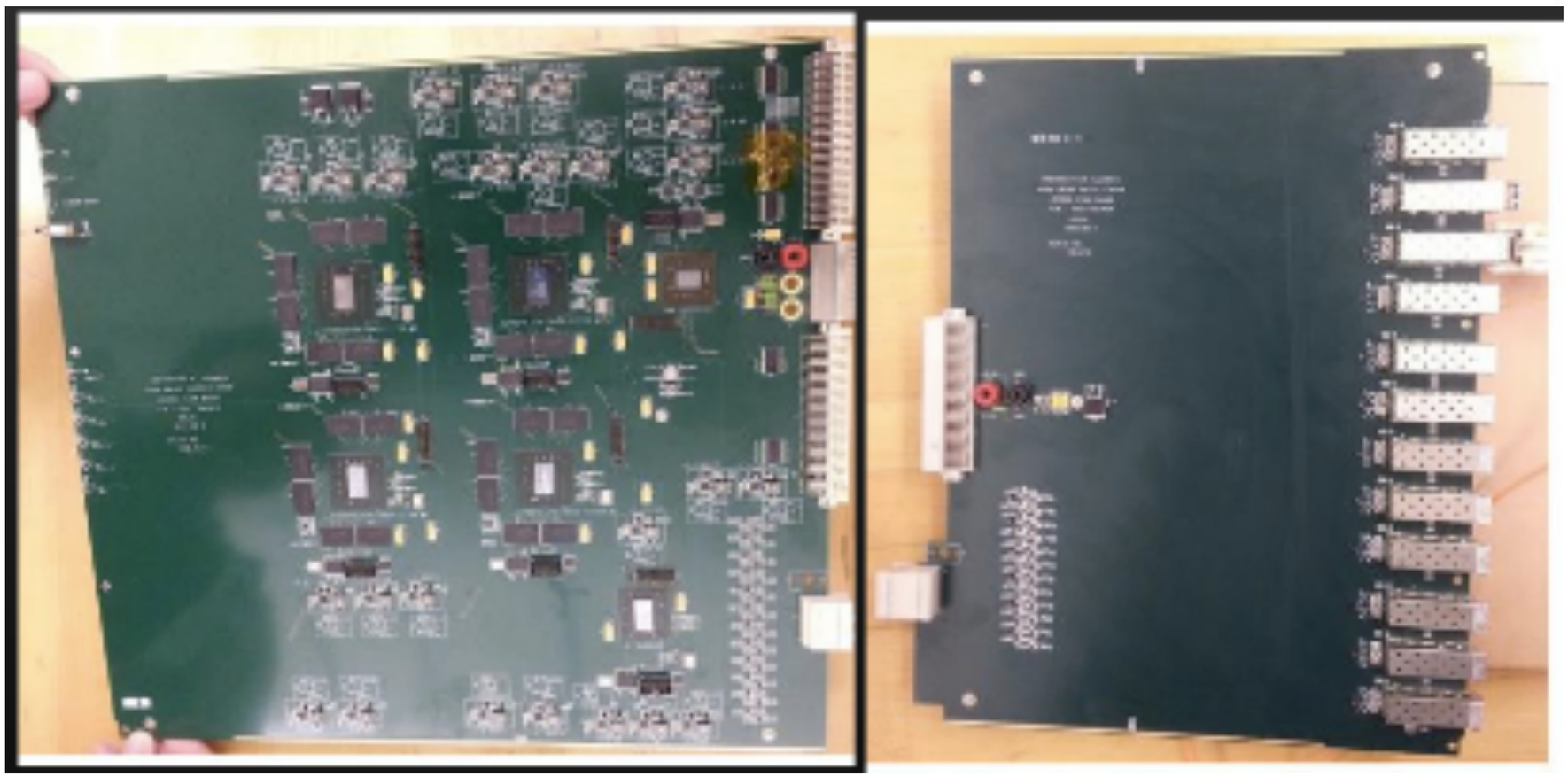




128 AUX boards are needed

SSB



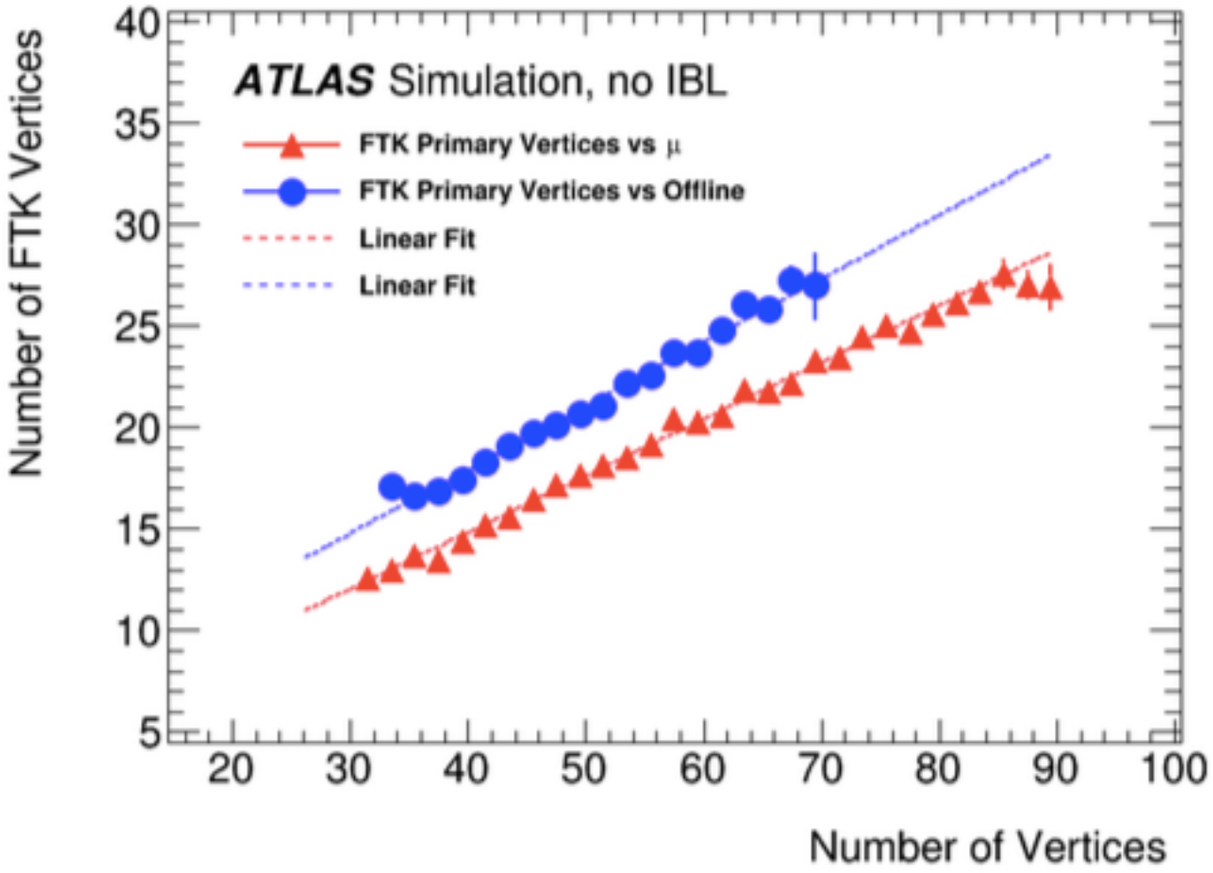


- Process received track candidates from the AUX cards and attempts to improve the precision with the additional hits from
  - 8 -layer tack is extrapolated to the 4 layers which were not used in the pattern matching
  - Uses linear approximation
  - Additional hits improve the track resolution and better reject the fakes
  - Remove duplicated tracks
  - Each SSB work with 2 towers -> 4AUX to 1 SSB
- The main board is provided of 6 FPGAs Xilinx Kintex 7, Large memory for track fitting constants.

32 SSB boards are needed

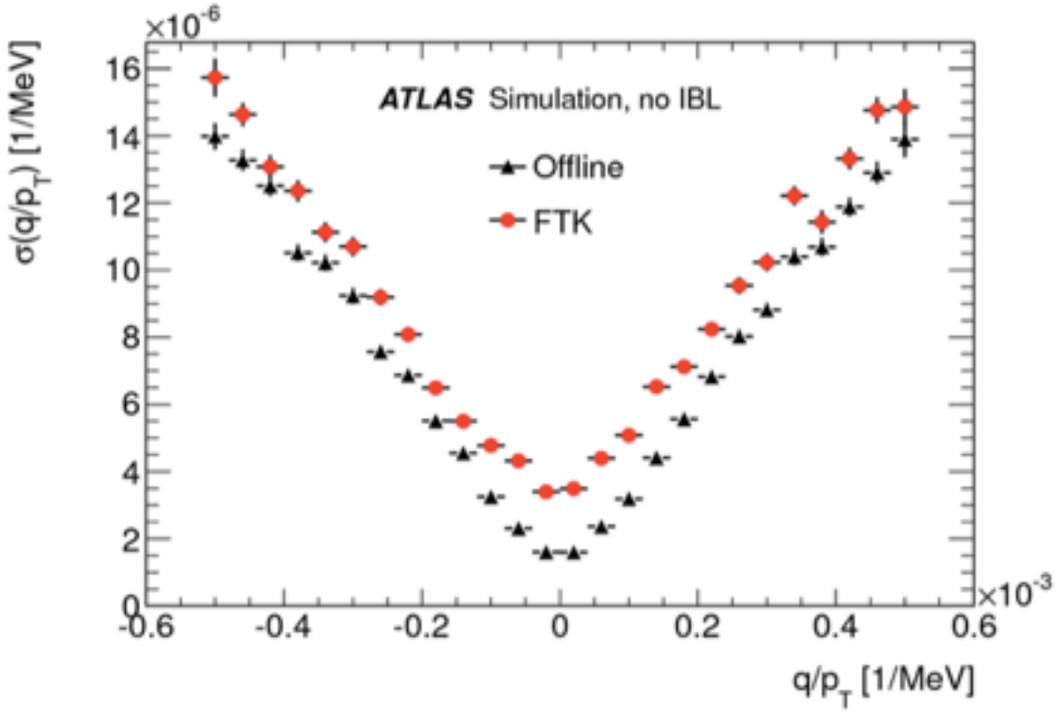
FTK simulations

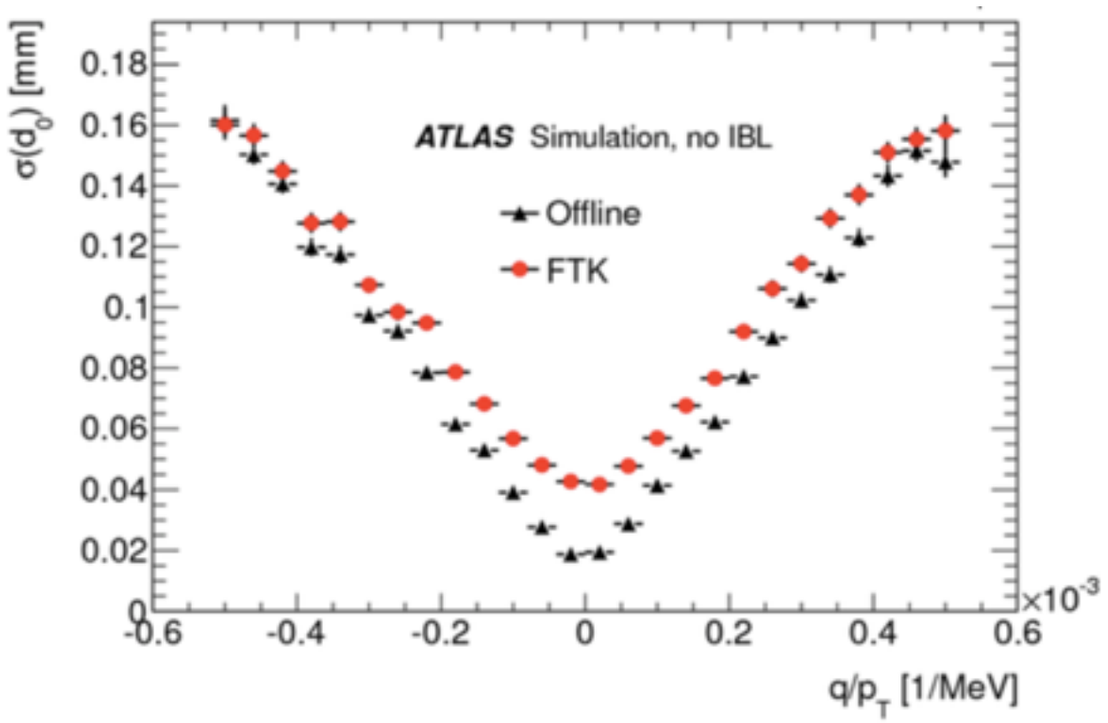
- Number of FTK and offline vertices have a linear correspondence
  - Independent of pileup

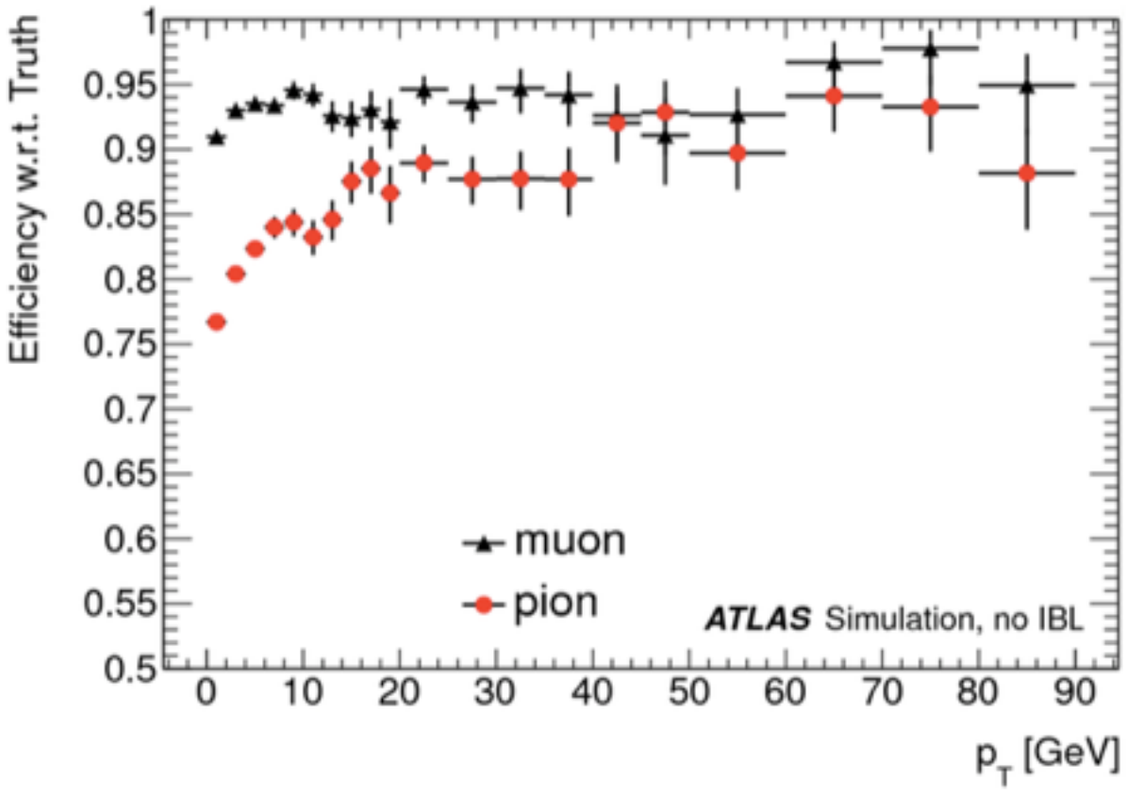


Vertexing

FTK simulations







Expected Efficiency