Phase-I Trigger Readout Electronics Upgrade of the ATLAS Liquid-Argon Calorimeters

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on behalf of the ATLAS Liquid Argon Calorimeter Group

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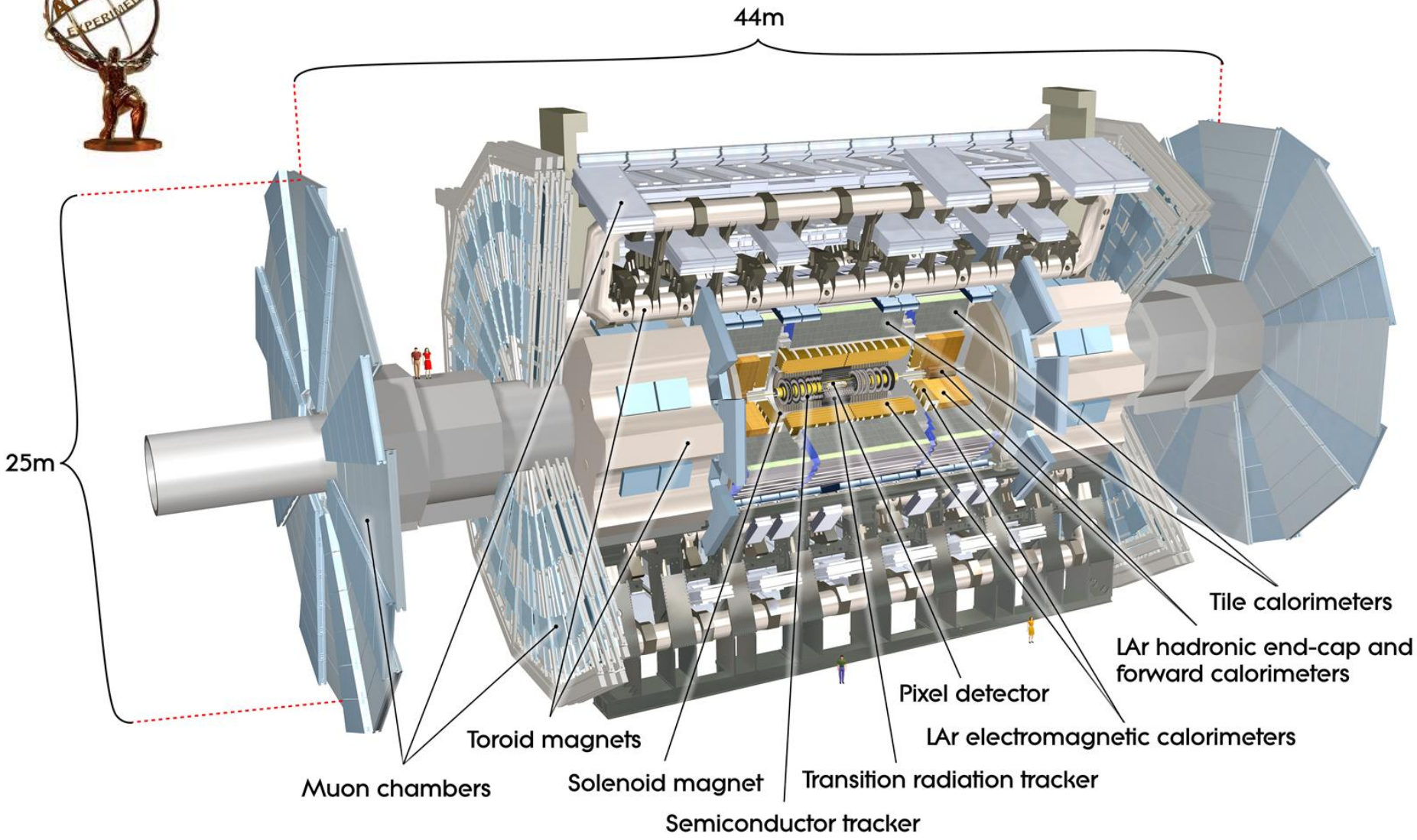
ATLAS LAr Calorimeter

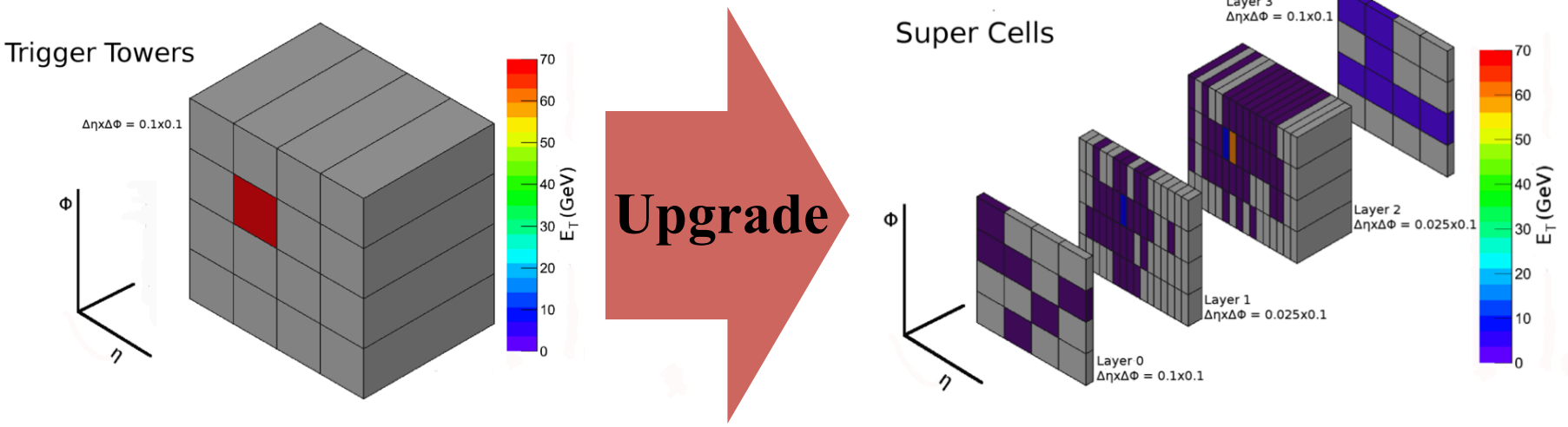
7000 tons
88 Million channels
3000 km of cables
2T solenoid
Toroid (B ~ 0.5T in barrel;~1T end-cap)



Phase I Upgrade of LAr Calorimeter Readout

Purpose :
providing higher-granularity, higher-resolution, and longitudinal shower information from the calorimeter to the Level-1 trigger processors

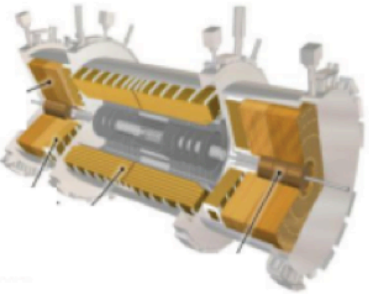
Strategy :
increasing granularity 10 times by changing from **Trigger Tower** to **Super Cell** readout (will be done during 2018)



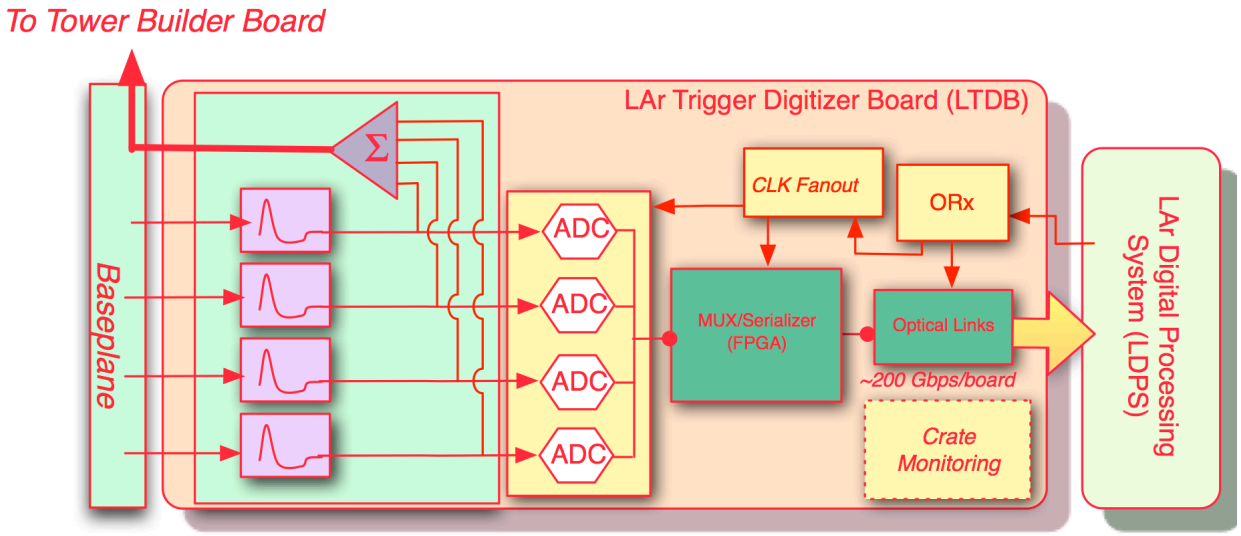
Trigger Tower :
sums the energy deposition across the longitudinal layers of the calorimeters in an area of $\Delta\eta \times \Delta\varphi = 0.1 \times 0.1$

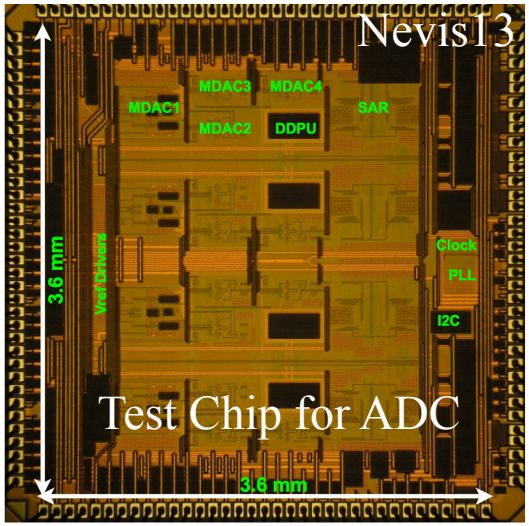
Super Cell :
provides information for each calorimeter layer for the full η range of the calorimeter, and finer segmentation ($\Delta\eta \times \Delta\varphi = 0.025 \times 0.1$) in the front and middle layers

The Architecture of Upgraded Trigger Electronics



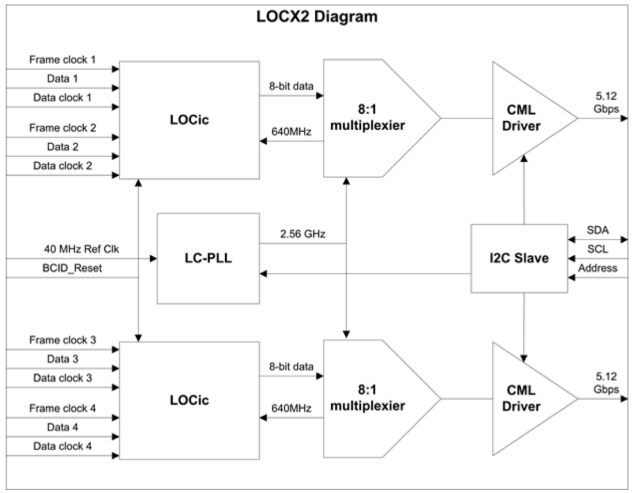
LAr Trigger Digitizer Board (LTDB)





The Role:

- receive analog signal and digitize Super Cell signals
  - Digitization is based on custom developed 12-bit SAR ADCs in 130 nm CMOS technology
    - 40 MHz sampling
    - radiation tolerance
- transmit the digitized signal to the back end
  - using the serializer (LOCx2) and optical driver (LOCld)
  - 5.44 Gb/s optical links per fiber (40 fibers in total)
- each of the 124 LTDBs handles up to 320 Super Cell channels



LAr Digital Processing System (LDPS)

The Role:

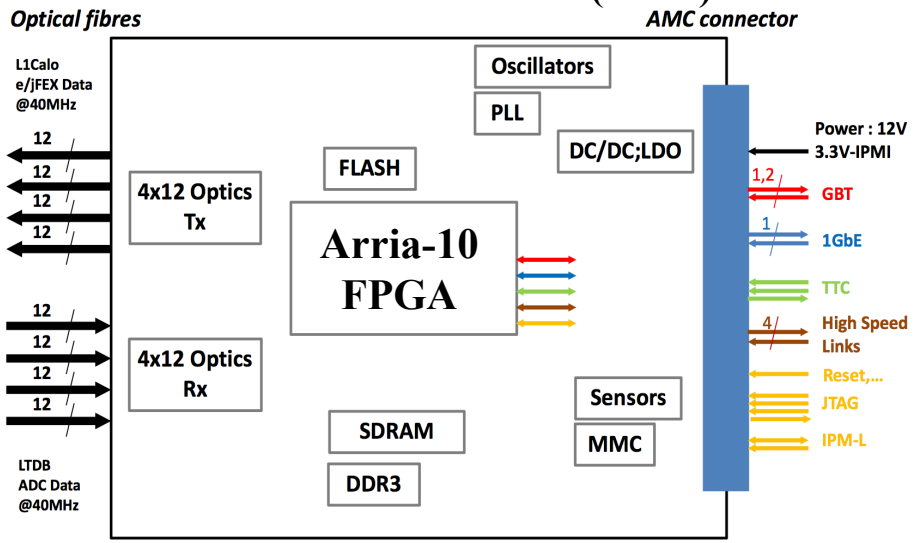
- receive the digitized data at a total rate of 25 Tb/s
- perform digital signal processing in real-time
- transmit the processed data to L1Calo at a total rate of 41 TB/s

Design of LDPS:

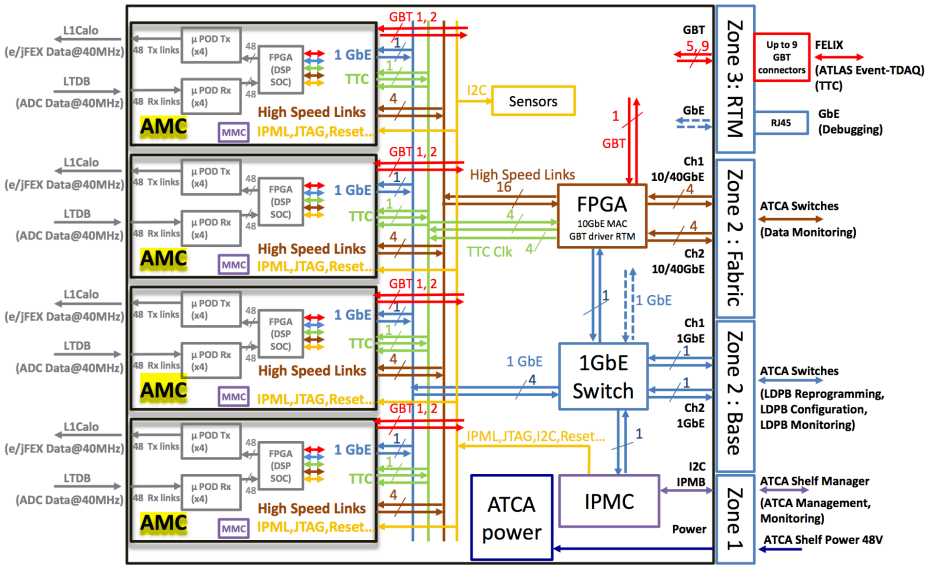
consist from 32 ATCA carrier blades

- which carry 4 mezzanine cards (AMC) each
- precise energy reconstruction, pile-up suppression and ID of the correct BC time are performed all on AMC
- real time processing done by ALTERA Arria-10
- each of which handles ~1100 Super-Cells on average

Advanced Mezzanine Card (AMC)



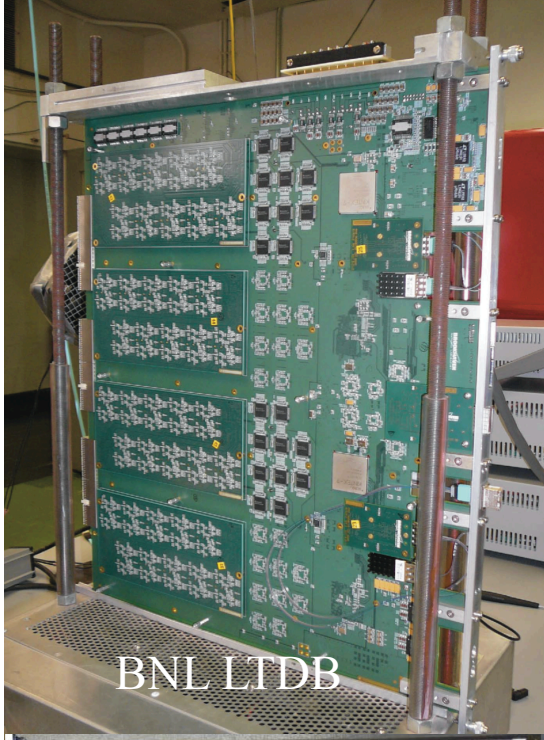
Carrier Board

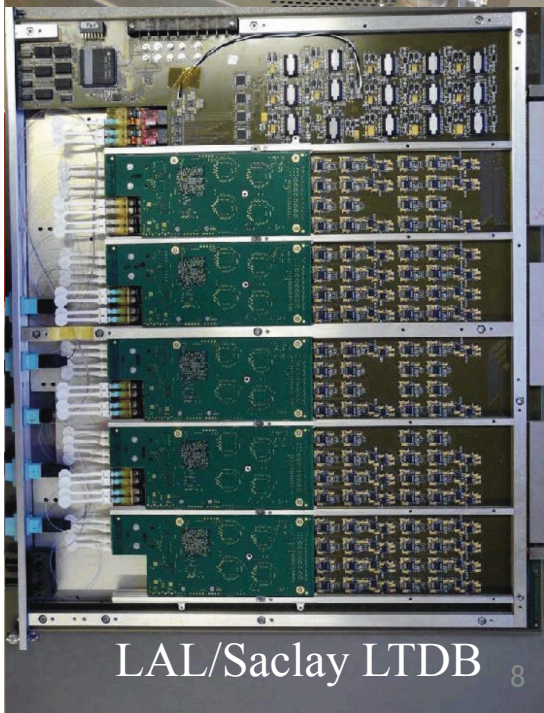


LTDB Demonstrator

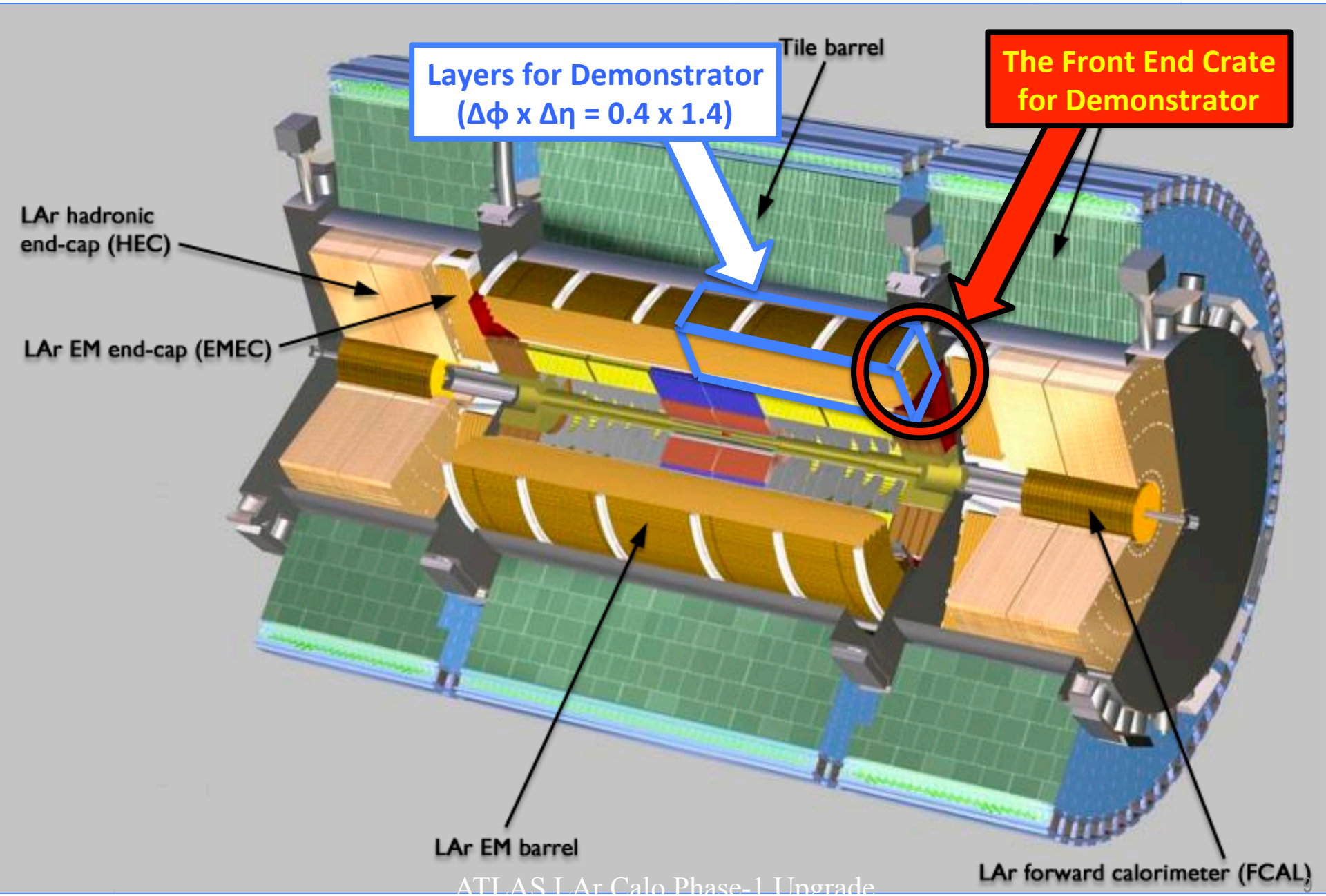
For testing the performance of the Super Cell,
LTDB Demonstrator has been installed
on the ATLAS detector (2014 Summer)

- installed in the barrel part ($1.767 < \varphi < 2.160$, $0 < \eta < 1.4$)
- operated in parallel to the regular ATLAS data taking during the LHC Run-2
- equipped with 2 prototype LTDBs (BNL, LAL/Saclay)
  - BNL : analog mezzanine, digital main board
  - LAL/Saclay : digital mezzanine, analog main board
  - ADC: TI ADS5272 for both cases
  - implement Stratix IV FPGAs
  - operated in a commercial Advanced Telecommunications Computing Architecture (ATCA) system


BNL LTDB


LAL/Saclay LTDB

Where Demonstrator is Installed



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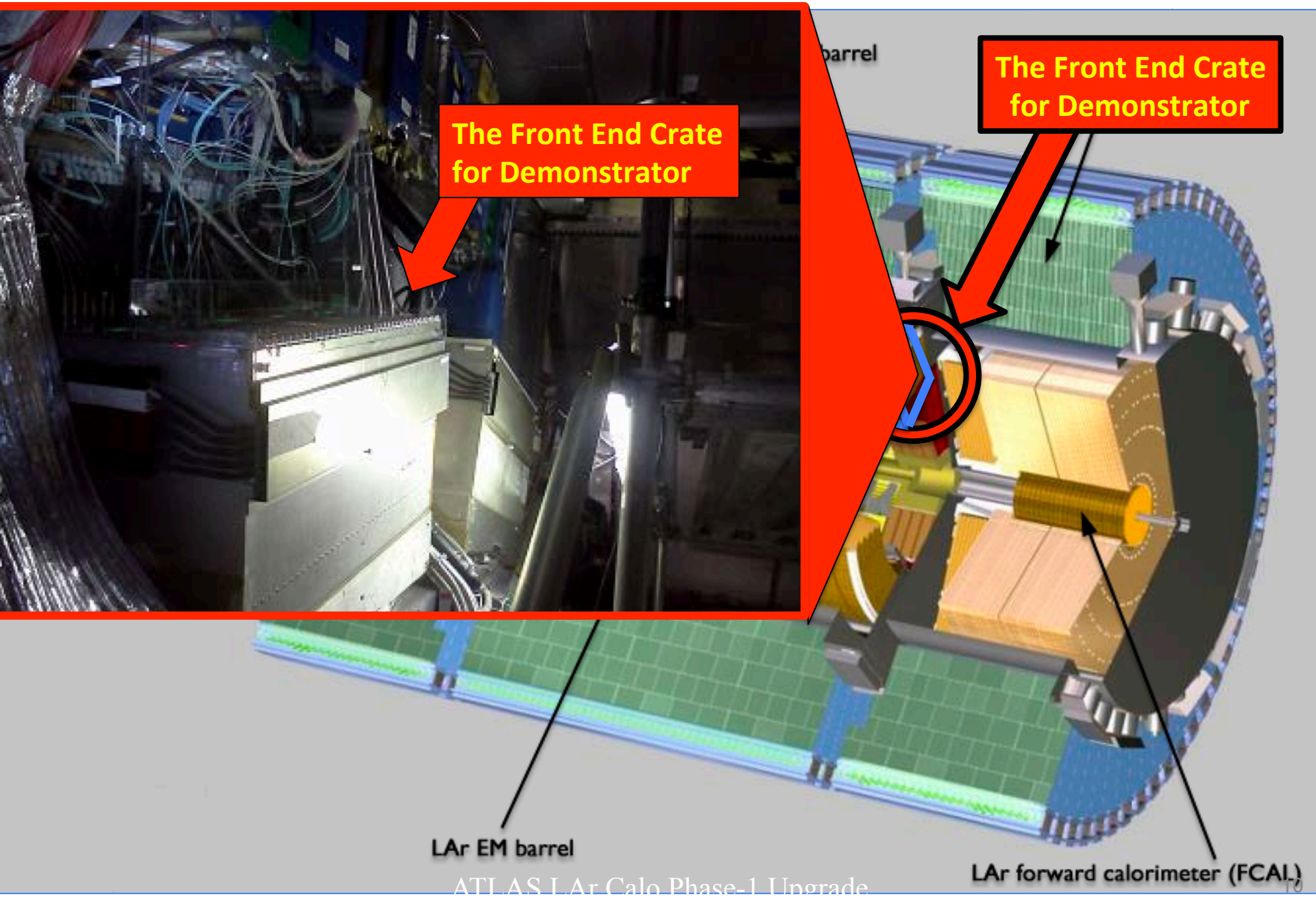

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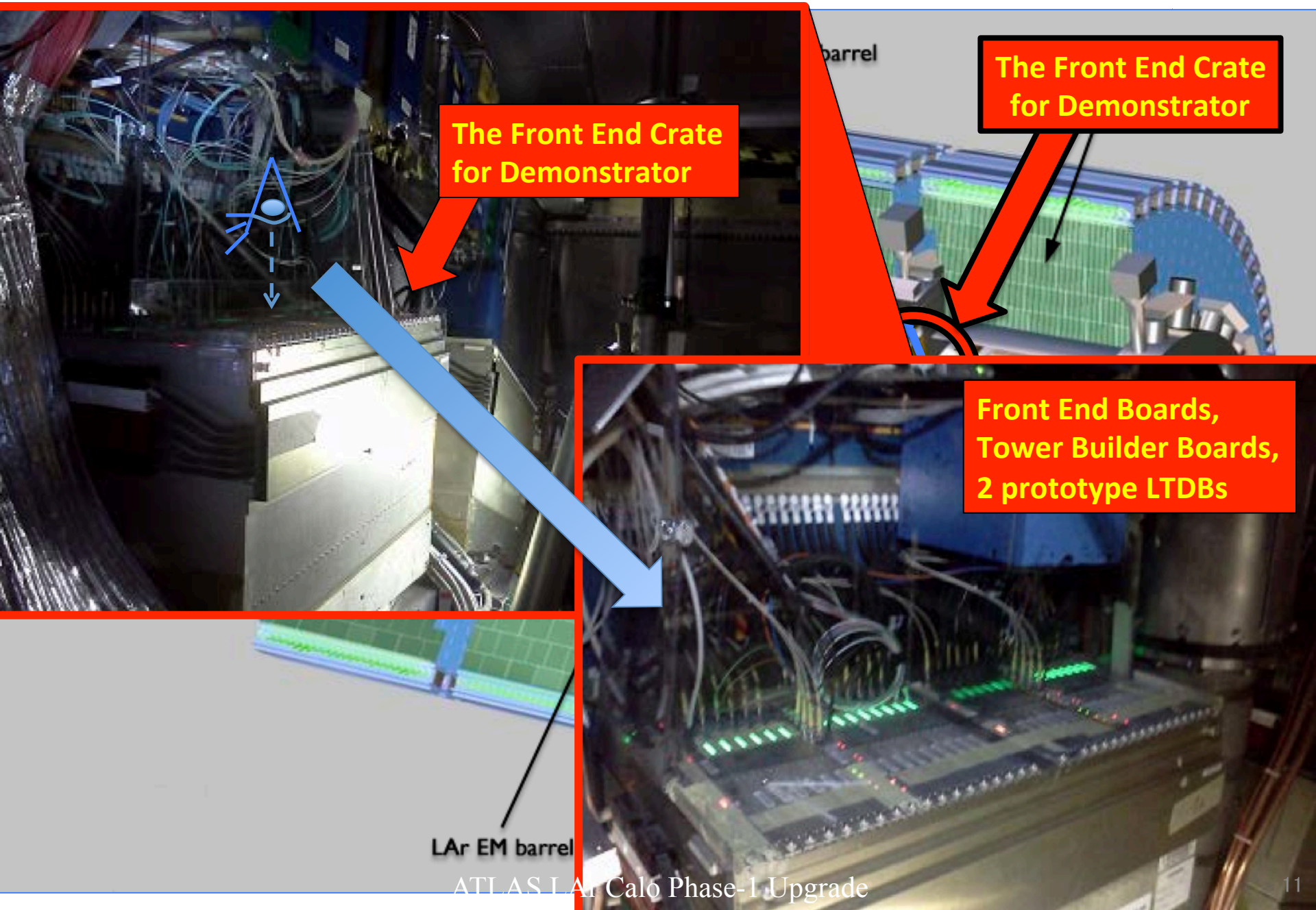
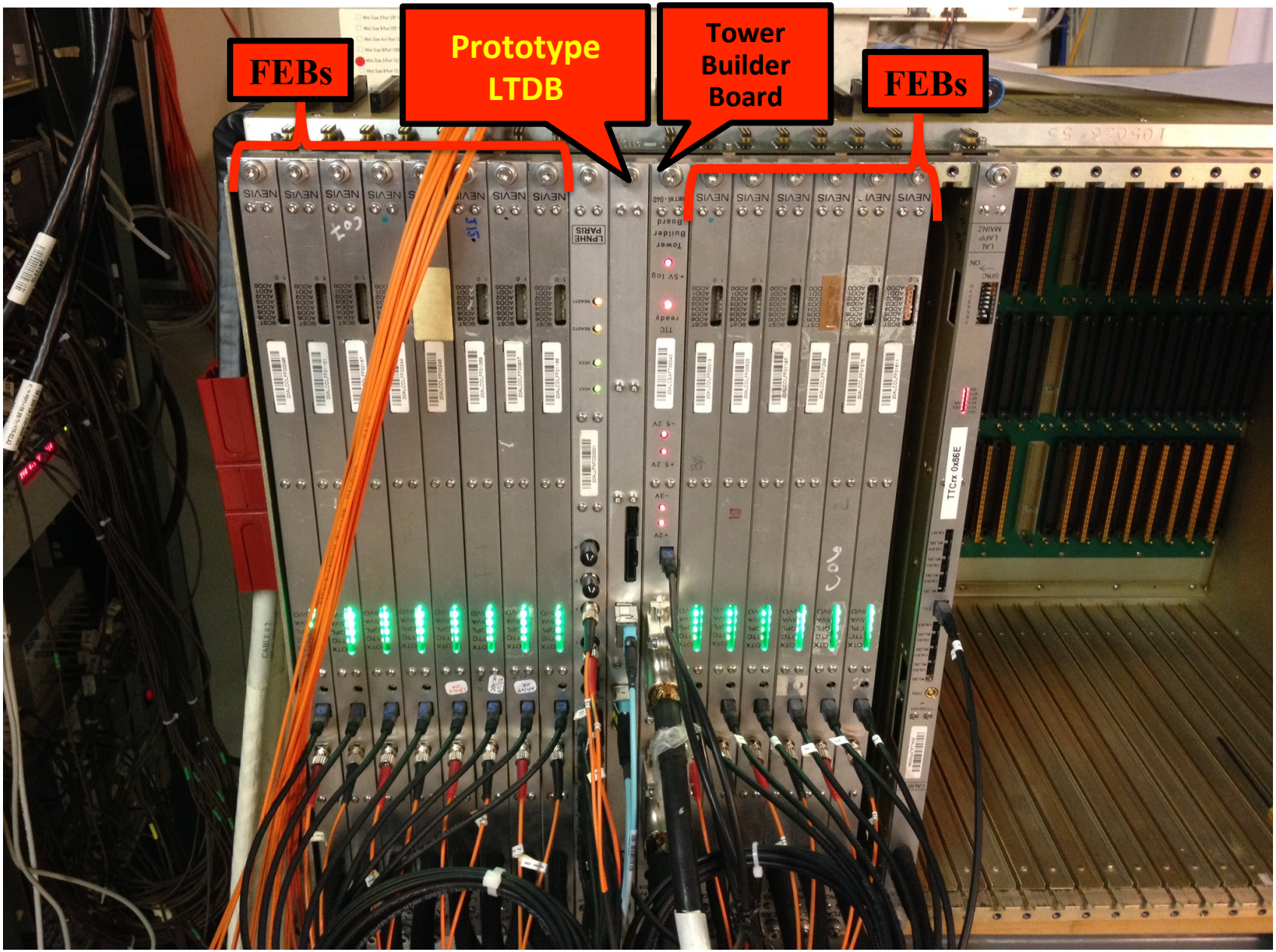


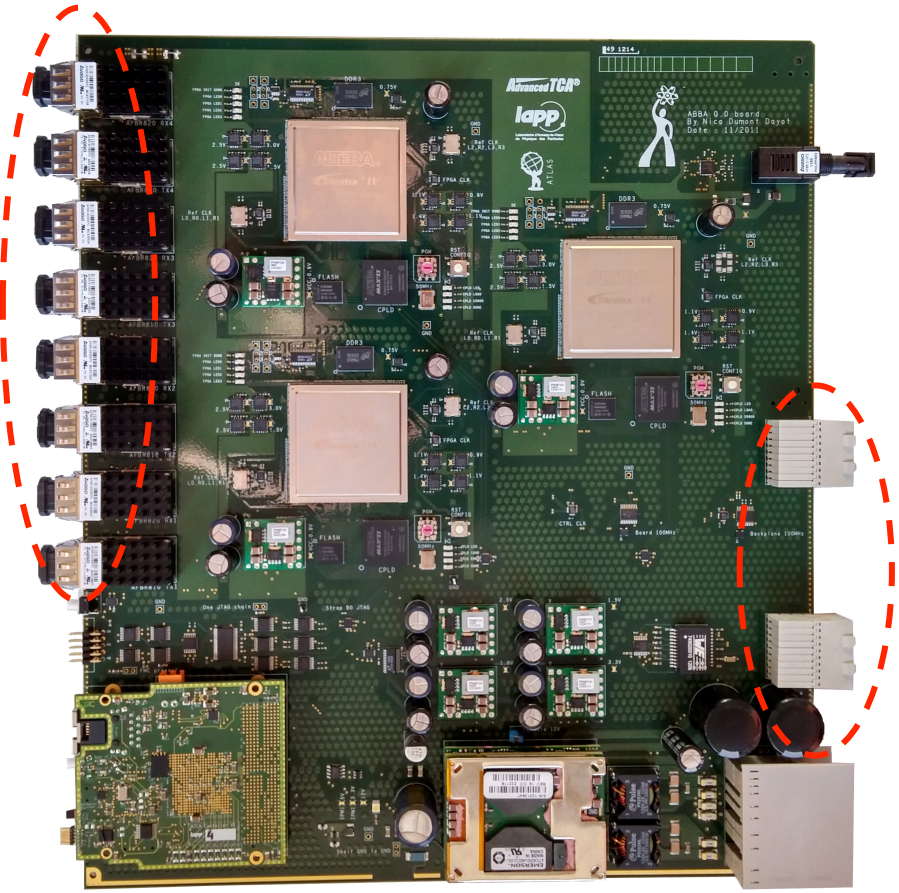
Front View of Demonstrator Crate



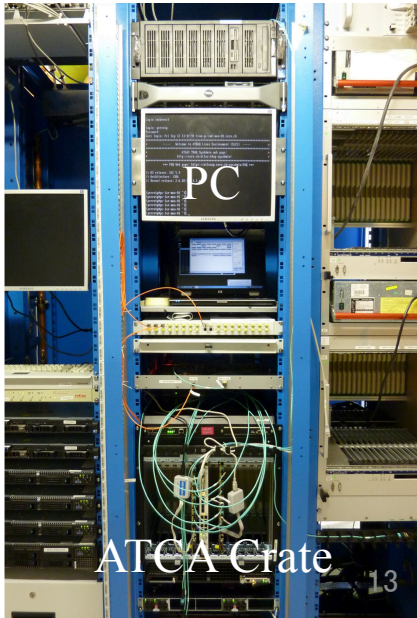
The Prototype LDPB on Demonstrator

- developed at LAPP
- The core components : ALTERA ® Stratix IV FPGAs
  - two Front FPGAs
    - receive digitized data
    - format them in ATLAS RAW Event Format
  - one Back FPGA
    - readout through ATCA fabric interface with IPbus
    - handle ICMP (Internet Control Message Protocol)
  - interconnected via XAUI

The optical transceivers from the LTDB



The connectors to a 10 GbE switch through ATCA backplane. The switch connected to PC with 2 optical fibers (TX/RX) at 10 GbE



ATCA Crate

Performance Results of Prototype Boards in the Demonstrator System

Measurements on Demonstrator System

On the legacy readout

- in order to verify no effect due to new electronics
  - Total Noise & Coherent Noise Fraction on Front End Boards
  - Total Noise on the Trigger Readout for Run2

On the demonstrator readout

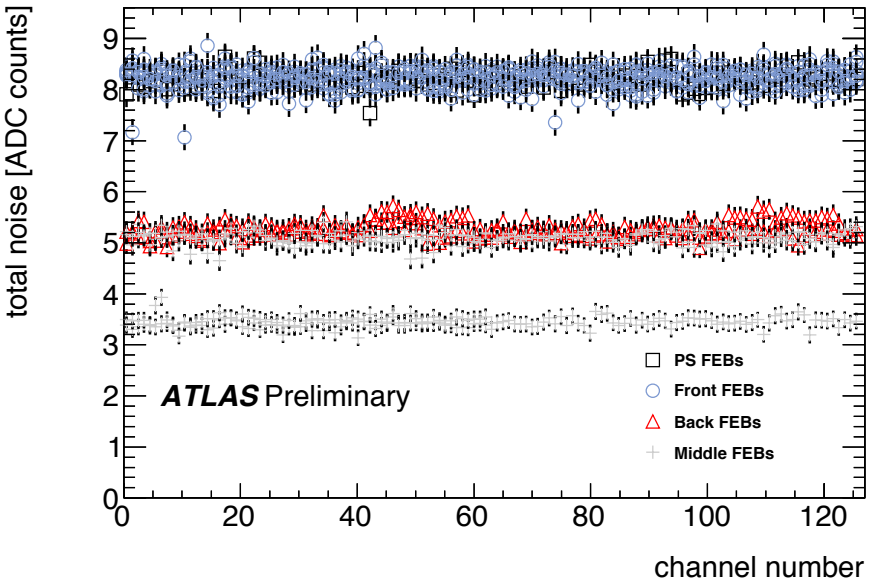
- Noise on LTDB Demonstrator
- Pulses from LTDB Demonstrator
- Linearity of LTDB Demonstrator

Total Noise on Front End Boards

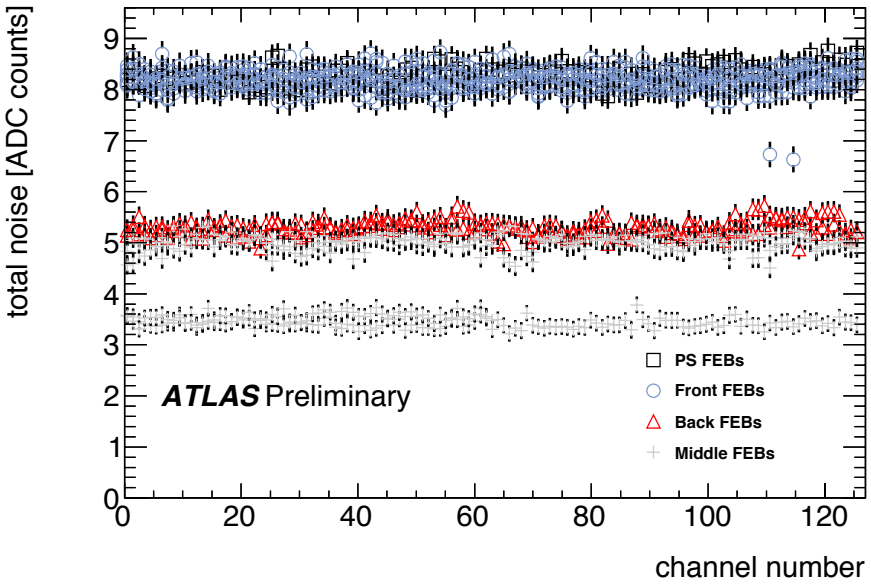
$$(\mathrm{TotalNoise})^2 \equiv \frac{\sum_k^{N_{evt}} (\sum_i^{N_{ch}} x_i^{(k)} - \sum_i^{N_{ch}} \mu_i)^2}{N_{evt}}$$

- The total noise of the 128 channels of the Front End Boards (FEBs)

demonstrator crate



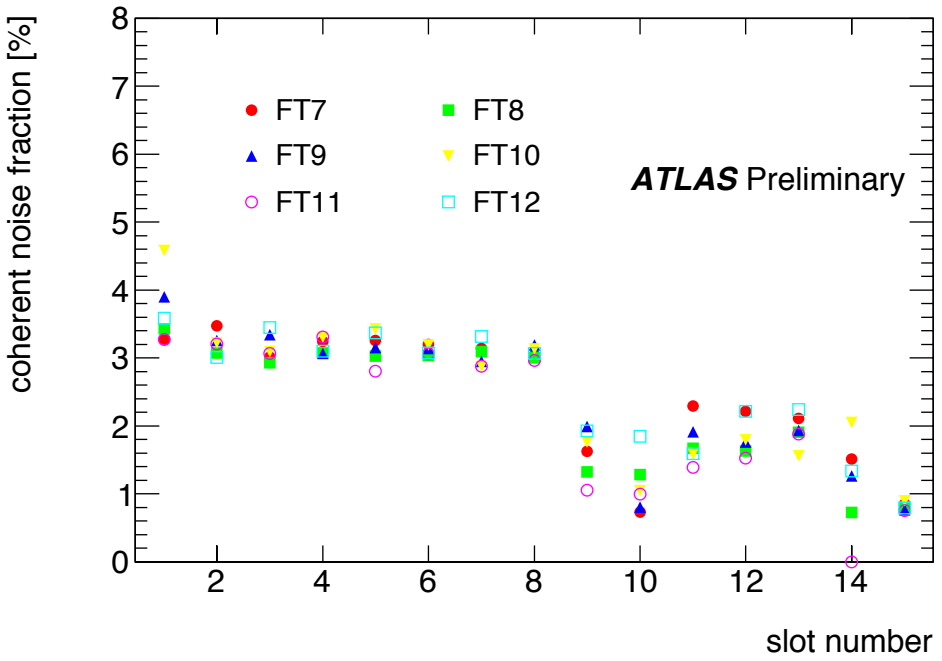
neighboring crate



→ The noise level of the demonstrator crate is consistent with that of neighboring crates

Coherent Noise Fraction on Front End Boards

- Coherent Noise Fraction (CNF : ρ_{COH}) indicates how much noise of a channel originates from coherent noise in average
- The CNF for feedthroughs (FT) 7-12 on the detector has been computed
  - FT9, 10 → demonstrator crate
  - FT7, 8, 11, 12 → neighbor crates



All channels in a FEB.

A channel in a FEB

$$\rho_{COH} = \frac{\sqrt{\sigma^2_{\sum_{i\in\mathcal{A}}} - N_{i\in\mathcal{A}} \cdot < \sigma^2_{i\in\mathcal{A}} >}}{N_{i\in\mathcal{A}} \cdot < \sigma_{i\in\mathcal{A}} >}$$

slot numbering

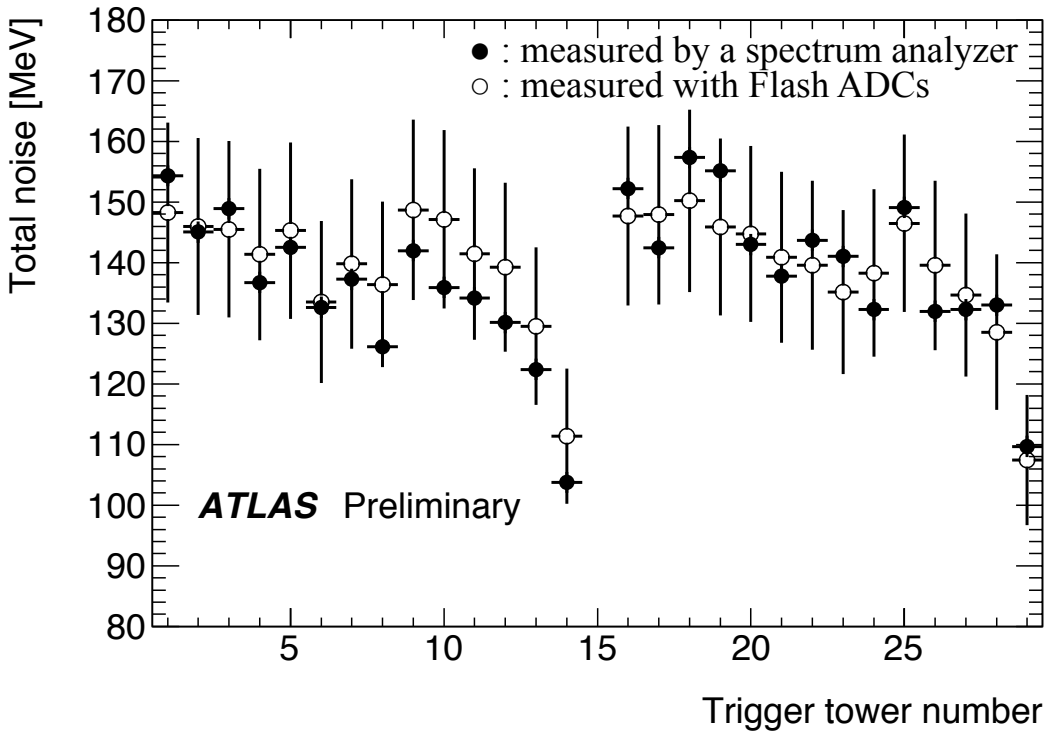
Layer	Pre-sampler	Front	Back	Middle	All
slot	1-2	3-8	9-10	11-14	15

→ The noise level of the demonstrator crate is consistent with that of neighboring crates

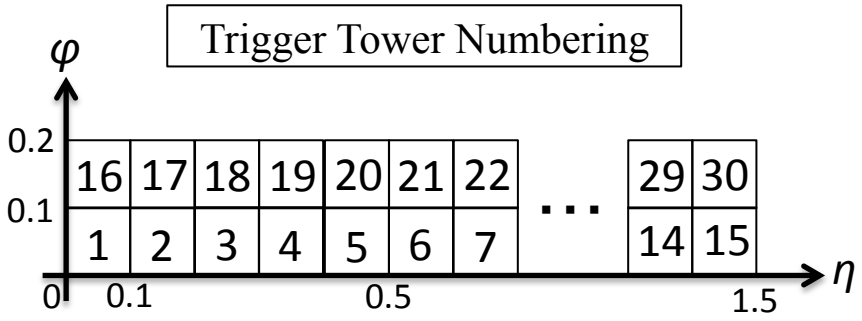
Total Noise on the Trigger Readout for Run2

- Total Noise on the Trigger Tower readout has been measured for confirming the demonstrator crate doesn't affect the trigger path used for physics @ Run2

$$(\mathrm{TotalNoise})^2 \equiv \frac{\sum_k^{N_{evt}} (\sum_i^{N_{ch}} x_i^{(k)} - \sum_i^{N_{ch}} \mu_i)^2}{N_{evt}}$$



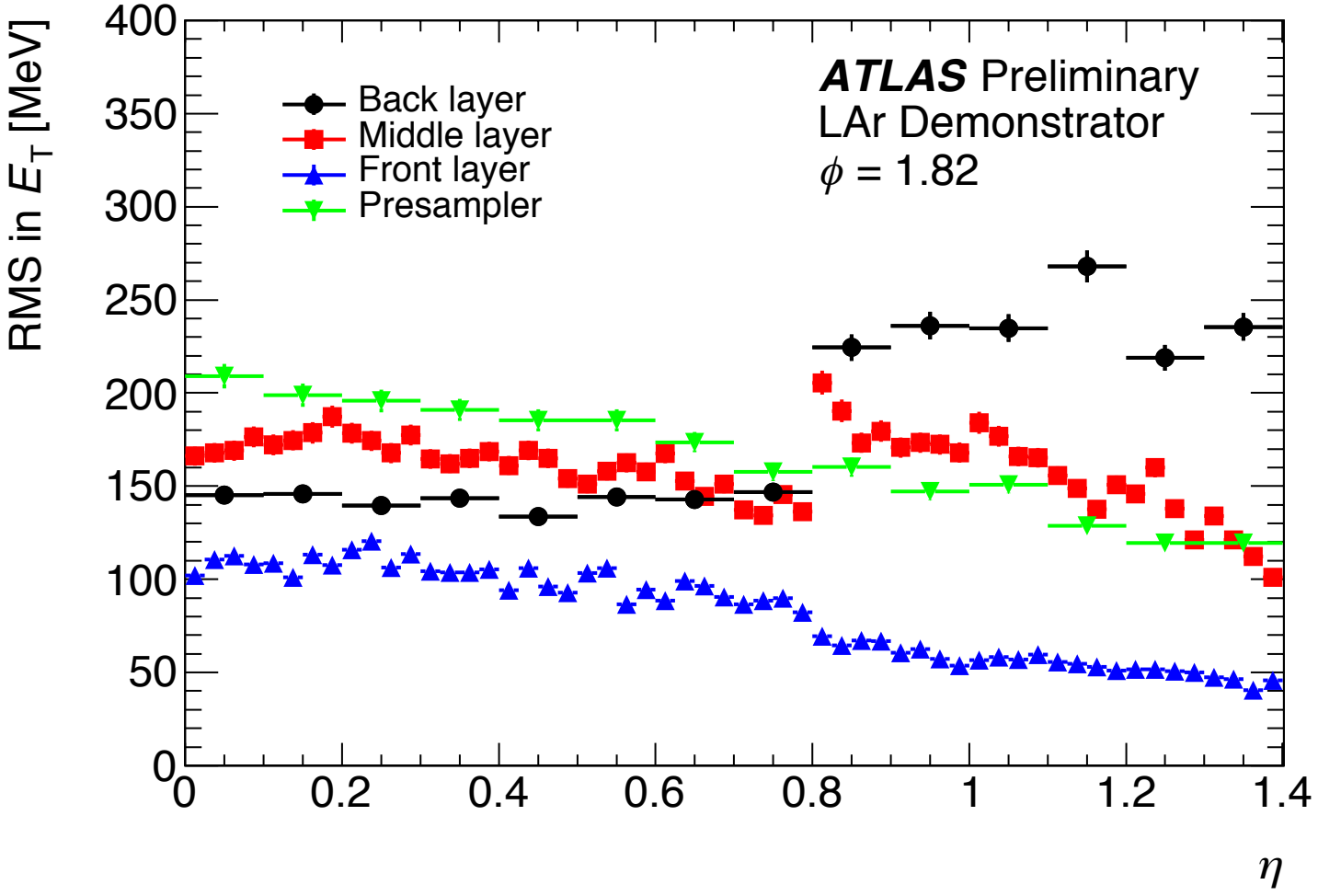
→Observed noise level is consistent with current system



On The Demonstrator Readout

Noise on LTDB Demonstrator

- RMS of pedestal ADC of LTDB Demonstrator has been measured

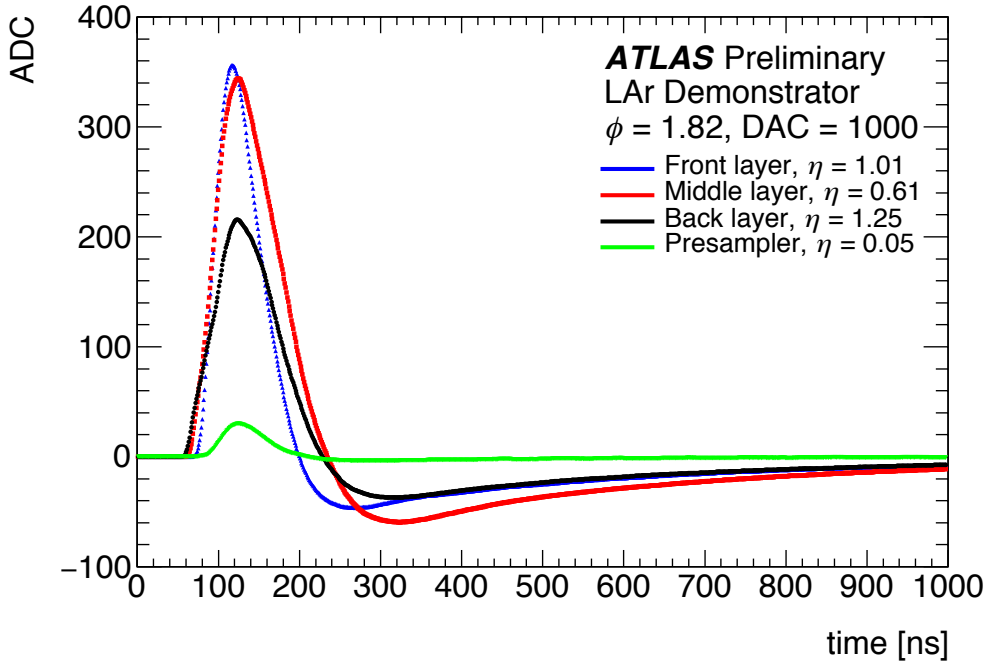


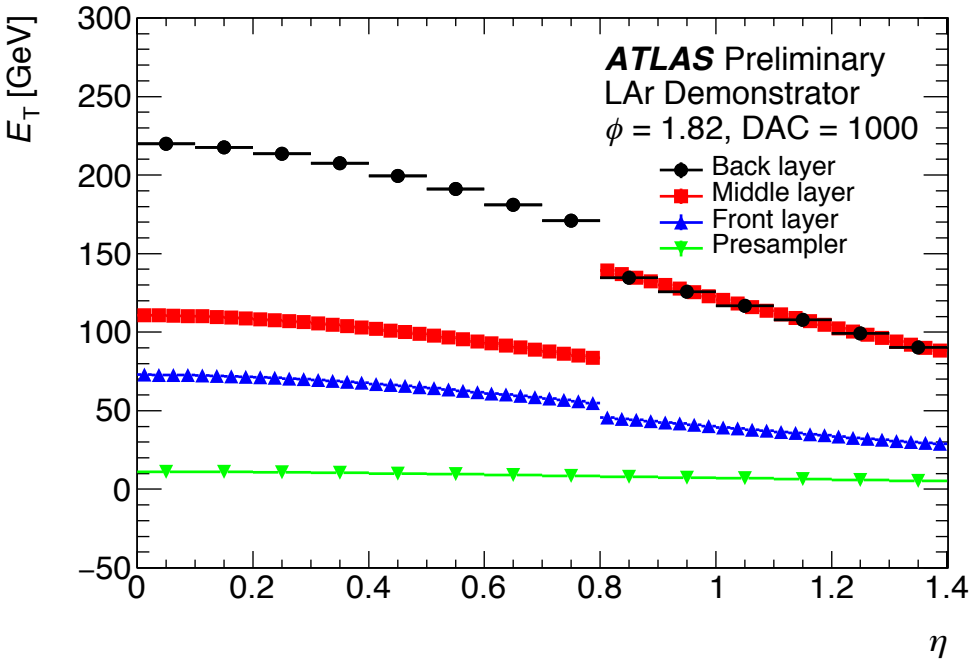
→The jump seen at eta=0.8 reflects the change of absorber thickness, electrodes and calibration resistors

Pulse from LTDB Demonstrator

- Pulses have been seen from LTDB Demonstrator

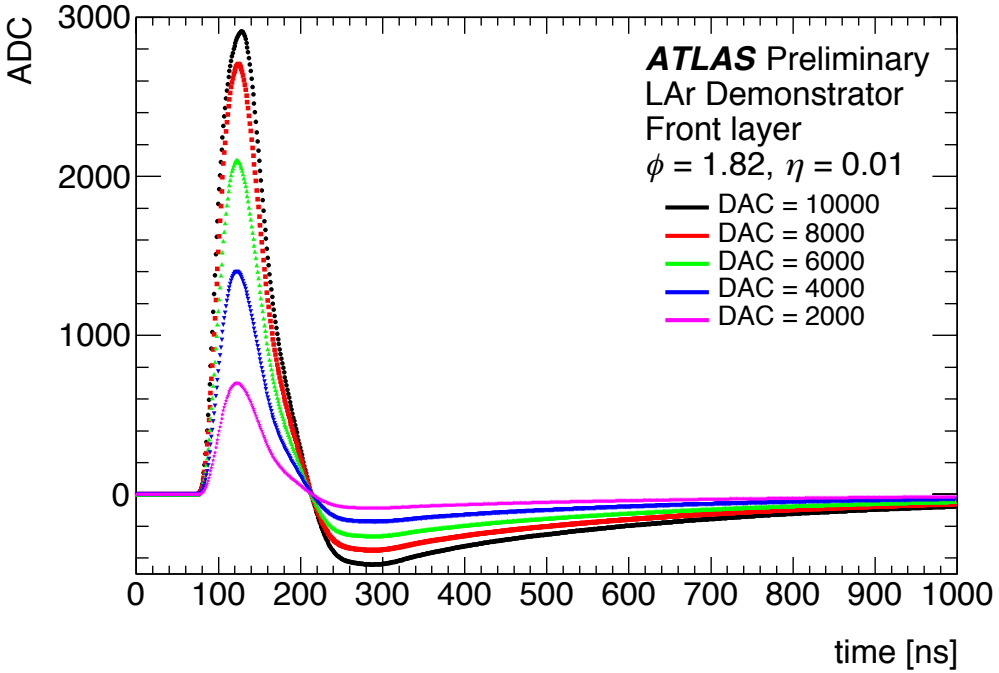
- $\Delta ADC \equiv ADC_{max} - ADC_{pedestal}$
  - $ADC_{pedestal}$ is defined by the average of pedestal values from 0 to 50 ns



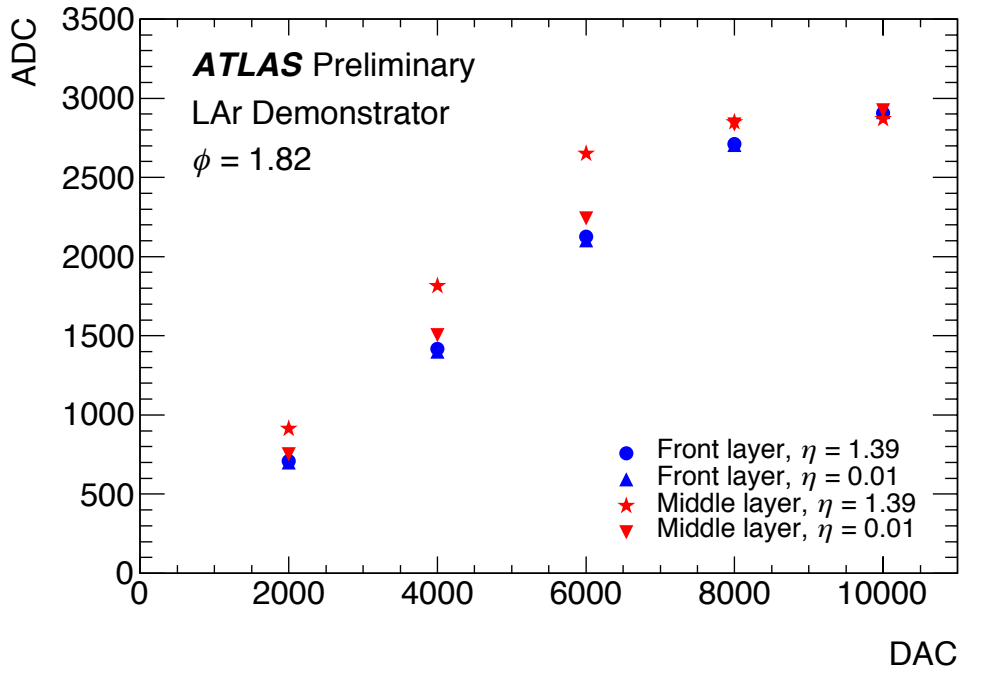


Linearity of LTDB Demonstrator

- Pulses have been checked with several DAC values



- Linearity has been checked as function of DAC
  - Red down-triangle corresponds to the upper plot
- ADC is saturated @ DAC = 10000, but ADC count is not saturated
  →already saturated at analog readout
  →expected & designed behavior



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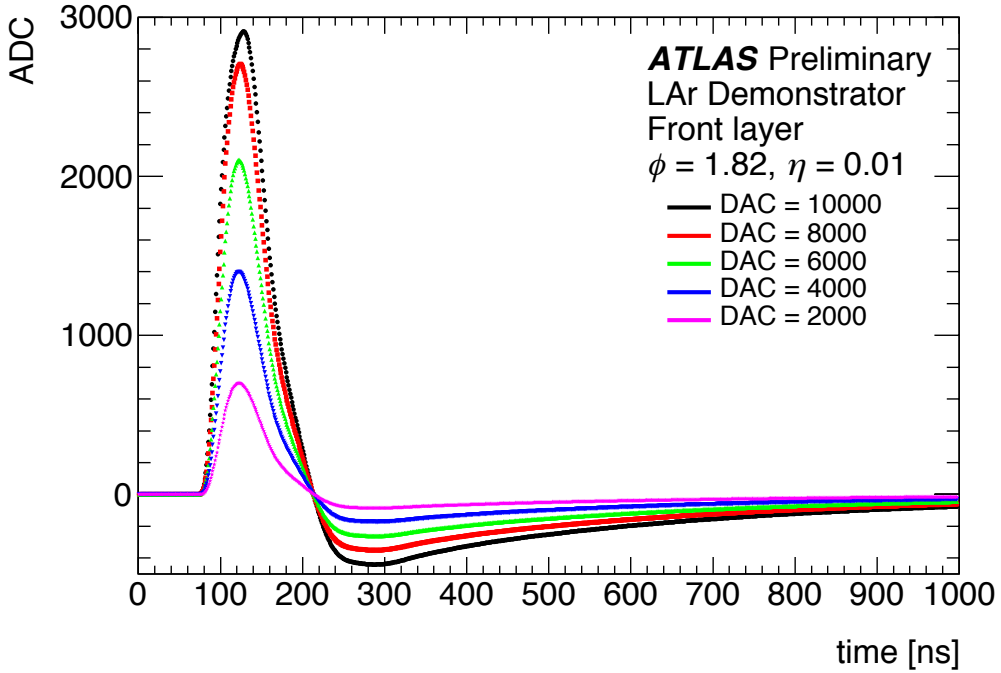
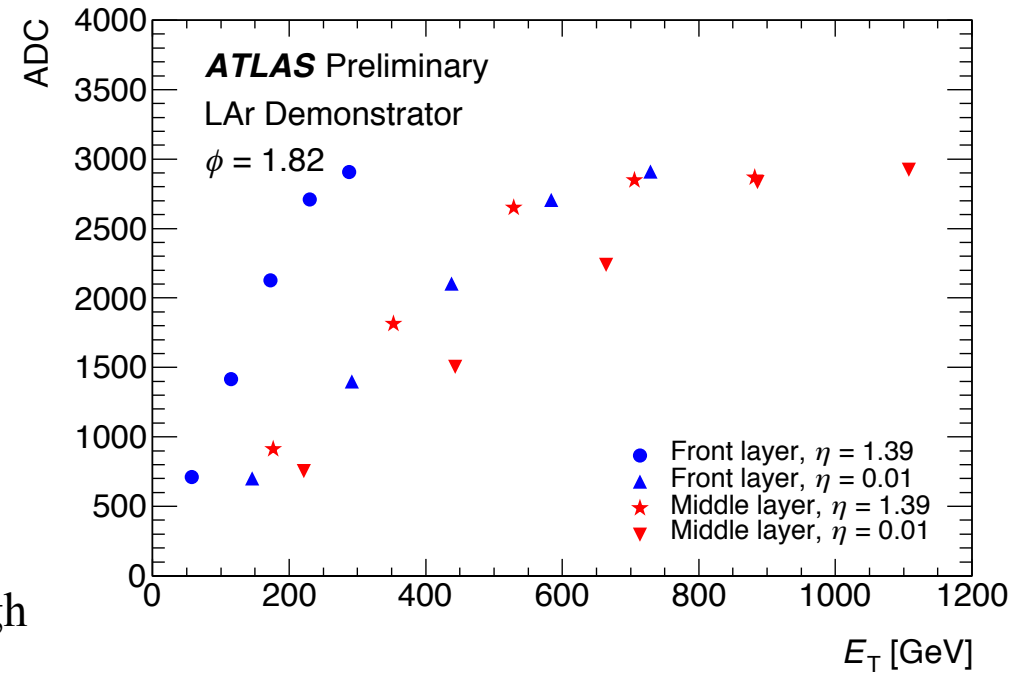


- Linearity has been checked as function of DAC
  - Red down-triangle corresponds to the upper plot
- ADC is saturated @ DAC = 10000, but ADC count is not saturated
  →already saturated at analog readout
  →expected & designed behavior
  →Linearity is kept up to high E_T enough



Summary

- The performance of the prototype LTDB & the prototype LDPB on the demonstrator system has been measured;
  - On the legacy readout
    - confirmed to have no significant noise
    - confirmed not to affect FEBs readout & trigger path for Run2 significantly
  - On the demonstrator readout
    - pulse and noise have been observed
    - linearity has been checked

Plan

- Take the following data with pp collision for filtering algorithm for energy reconstruction
  - Response of real EM object
  - Noise data

  → These are data for filtering algorithm development which we can not get without the demonstrator

Thank you very much!

Backup

The Upgraded Trigger Electronics