## FRONT-END ELECTRONICS FOR TPC MPD/NICA

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**TPC/MPD** Collaboration

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### CONTENS

- Introduction (MPD setup, TPC design overview and general characteristics)
- Main parameters and base of the FEE TPC
- FEE prototype
- Testing of FEE
- FEE for one readout chamber
- Conclusions

### General view of the MultiPurpose Detector (MPD) NICA project

- SC Coil superconductor solenoid
- IT inner detector
- ECT straw-tube tracker
- TPC time-projection chamber
- TOF time-of-flight stop counters
- FD The fast forward detectors
- ZDC zero degree calorimeter
- BBC beam-beam counter



3

### TPC design overview



#### **Physics requirements:**

The overall acceptance on  $|\eta| \sim 1.2$ 

The momentum resolution ~ 3% in  $p_t$  interval from 0.1 to 1 GeV/c

Two-track resolution ~ 1 cm.

Charged particle multiplicity ~ 1000 in a central collisions

Hadron and lepton identification by dE/dx measurements with resolution better than 8%

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### Main parameters of the FEE TPC

Significant data volume makes a special demands to the FEE. Electronics is designed with a modern technologies.

- ✓ Total number of channels 95 232
- $\checkmark$  Mean data stream from whole TPC 10 GB/s
- ✓ Low power consumption less then 100 mW/ch
- ✓ Fast optical transfer interface
- $\checkmark$  Based on ASIC and FPGA

### Block diagram of FEE base



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6

### Front-End Electronics prototype

#### FEC-64 channels



Signal to noise ratio, S/N - 30
σ<sub>NOISE</sub> < 1000e<sup>-</sup> (C=10-20 pF)
Dynamic Range - 1000

- Zero suppression
- Buffer (4 / 8 events)

ALTERA FPGA - board control

FTDI USB2.0 (prototype only)

4 PASA chip 16 channels ASIC (low noise amplification of the signal)

4 ALTRO chip 16 channels ASIC (digitization and signal processing)

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## FECs stress tests and debugging FPGA firmware

Main functionality tests were performed during 3 months at 8 hours per day.

The following operation conditions are tested:

- «With baseline correction»;
- «Without zero suppression» (big event volume);
- Trigger rate variate from 10 Hz to 3 kHz;
- With number of ALTRO buffers from 1 to 8;
- «Stream mode»;
- «Receive event after event»;

Event real-time checking (less then 0.3 % of errors);

# Testing FECs on the test bench with signal generator



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## Testing of 3 FECs on readout chamber prototype



Readout chamber prototype

 $\gamma$  quantum value with energy E= 6 kEv which fell on the middle of pad 36

- Trigger from anode wires
- γ quantum ~ 400 Hz
- Total number of channels 64x3
- Event collection with different collimators



### FEE Testing





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### FEE for one readout chamber

Readout control unit prototype based on the ALTERA Cyclone V SX SoC Development Board

Cyclone V 5CSXFC6D6F31C6N Chip with high-speed transceivers and embedded HPS

1Gb/s Ethernet

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High-speed transceiver 2.5 Gb/s

### Future possible improvement

- New ASIC chip is under development in CERN
- ALICE and STAR have FEE upgrade projects based on that ASIC
- Dubna team is participating in chip testing to understand its feasibility for NICA TPC FEE

### Conclusion

- ✓ Base FEE concept was developed
- 6 Prototype cards have been designed, produced & tested
- ✓ New FECs was designed
- ✓ Testing and debugging of new cards is ongoing
- RCU prototype based on ALTERA Cyclone V dev. board is almost finished
- ✓ We consider deferent ways to improve our system

I'd like to thanks for help:

### Alexander Moskovsky (JINR) Alexander Pilyar (JINR)

### Thank you for your attention!

### Main parameters of the TPC

Length of the TPC 340 cm Outer radius of cylinder 140 cm Inner radius of cylinder 27 cm Length of the drift volume 170cm (of each half) Magnetic field strength 0.5 Tesla Drift gas 90% Ar+10% CH<sub>4</sub> 0.5°C **Temperature stability** Gas amplification factor ~ 10<sup>4</sup> Number of readout chambers 24 (12 per end plate) Pad size 5x12mm<sup>2</sup> and 5x18mm<sup>2</sup> Number of pads 95 232 Pad raw numbers 53 ~5 kHz Maximal trigger rate dE/dx better than 8% ~ 3% in 0.1< p,<1 GeV/c ∆p/p