READOUT ELECTRONICS FOR TPC MPD/NICA

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- **FEE prototype (FEC-64)**
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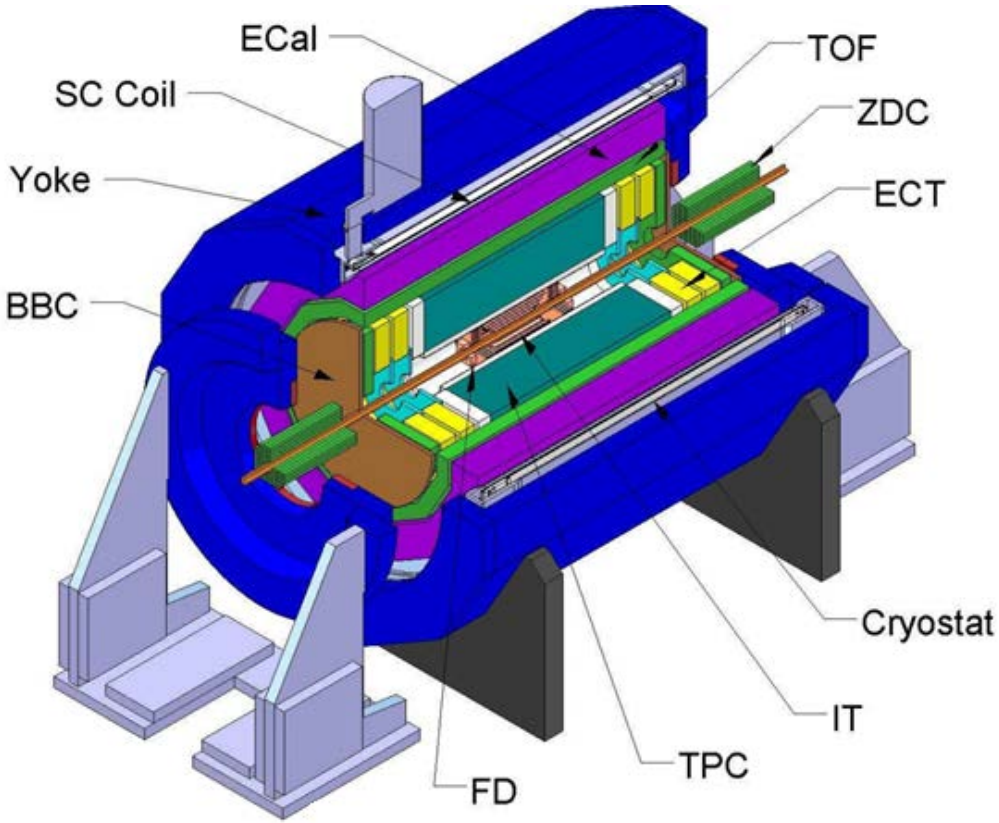
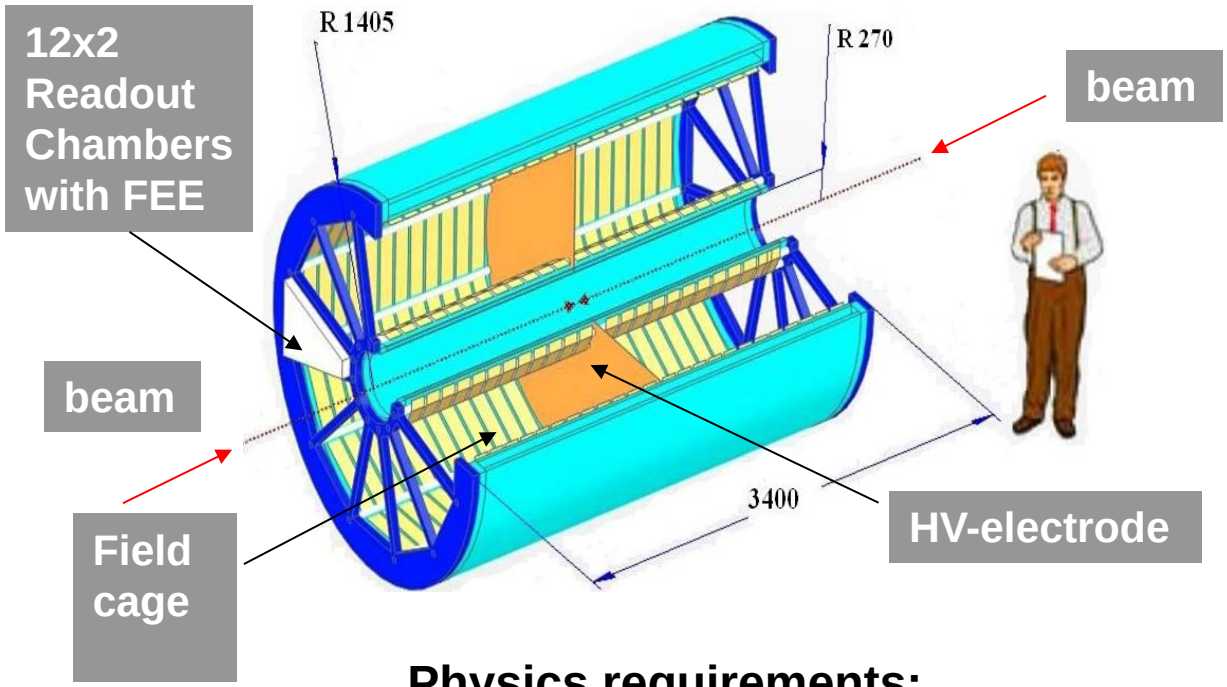
- **Conclusions**

GENERAL VIEW OF THE MPD DETECTOR



- SC Coil - superconductor solenoid
- IT - inner detector
- ECT - straw-tube tracker
- TPC - time-projection chamber
- TOF - time-of-flight stop counters
- FD - fast forward detectors
- ZDC - zero degree calorimeter
- BBC - beam-beam counter

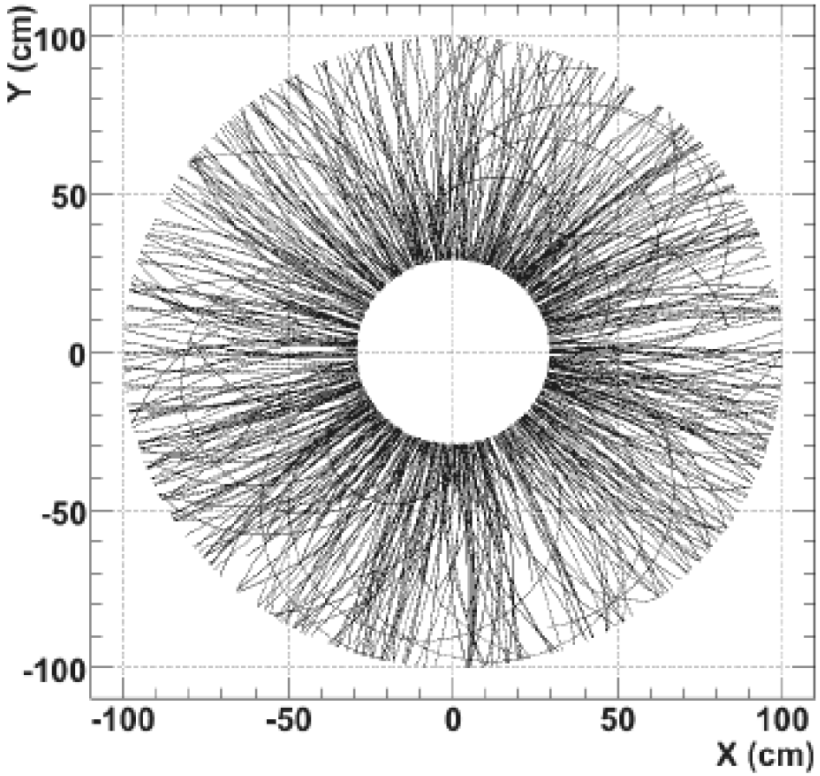
TPC DESIGN OVERVIEW



Physics requirements:

The overall acceptance on $|\eta| \sim 1.2$
The momentum resolution ~ 3% in p_t interval from 0.1 to 1 GeV/c at 0.5 Tesla
Two-track resolution ~ 1 cm.
Charged particle multiplicity ~ 1000 in a central collisions Au + Au
dE/dx - better than 8%

SIMULATION RESULTS



UrQMD model simulation

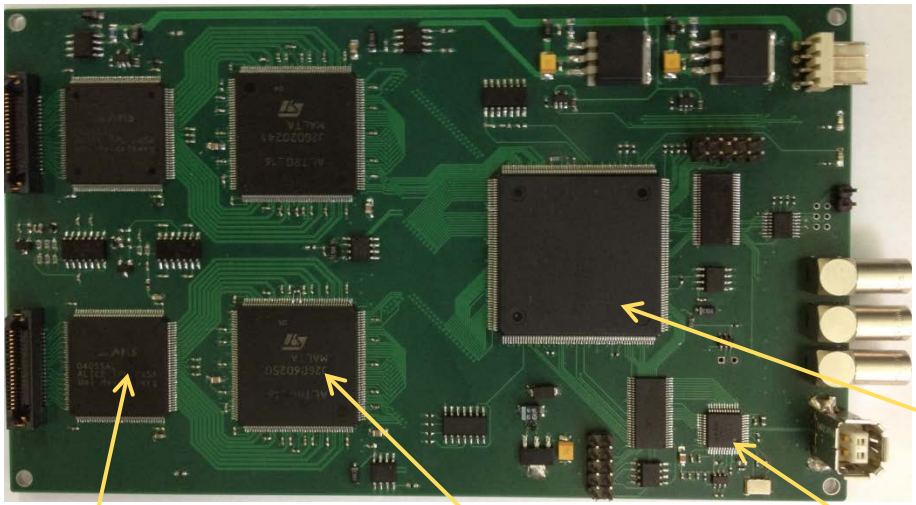
TPC/MPD, central Au + Au collision at 9GeV

MAIN PARAMETERS OF THE FEE TPC

- ✓ **Total number of channels - 95 232**
- ✓ **Data stream from whole TPC – 5 GB/s**
- ✓ **Low power consumption – less then 100 mW/ch**
- ✓ **Fast optical transfer interface**
- ✓ **Based on ASIC and FPGA**

FRONT-END ELECTRONICS PROTOTYPE

FEC-64 channels



- Signal to noise ratio, S/N - 30
- $\sigma_{NOISE} < 1000e^-$ (C=10-20 pF)
- Dynamic Range - 1000
- Zero suppression
- Buffer (4 / 8 events)

PASA chip
16 channels ASIC
(low noise amplification of the signal)

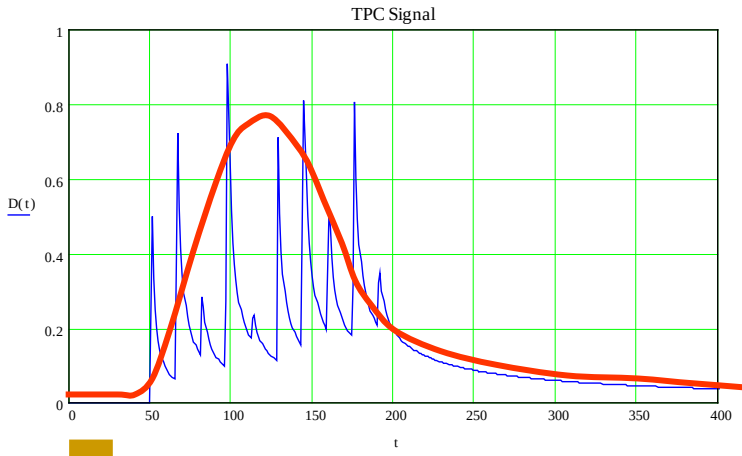
ALTRO chip
16 channels ASIC
(digitization and signal processing)

ALTERA FPGA - board control

FTDI USB2.0
(prototype only)

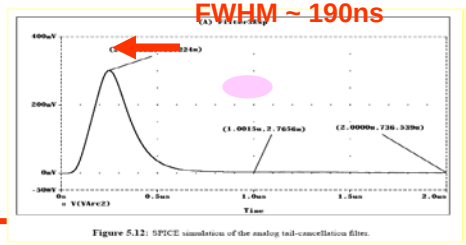
PROCESSING IN PASA & ALTRO

- FWHM – 190ns
- Baseline restoration after 1μs:
  - ~ 5 % in amplifier / shaper
  - ~ 0.1% in dig. chip



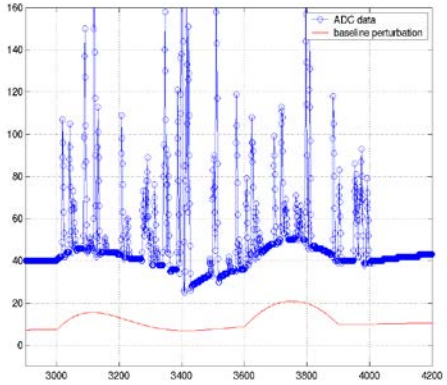
PASA

FWHM ~ 190ns

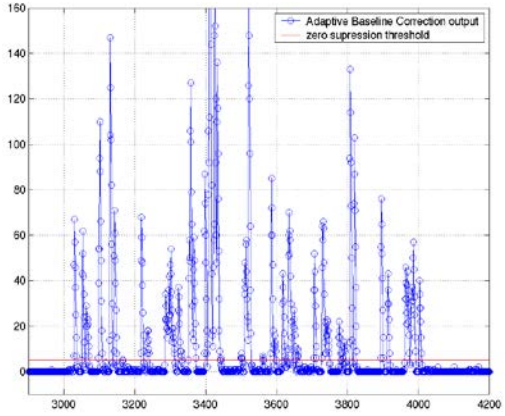


ALTRO

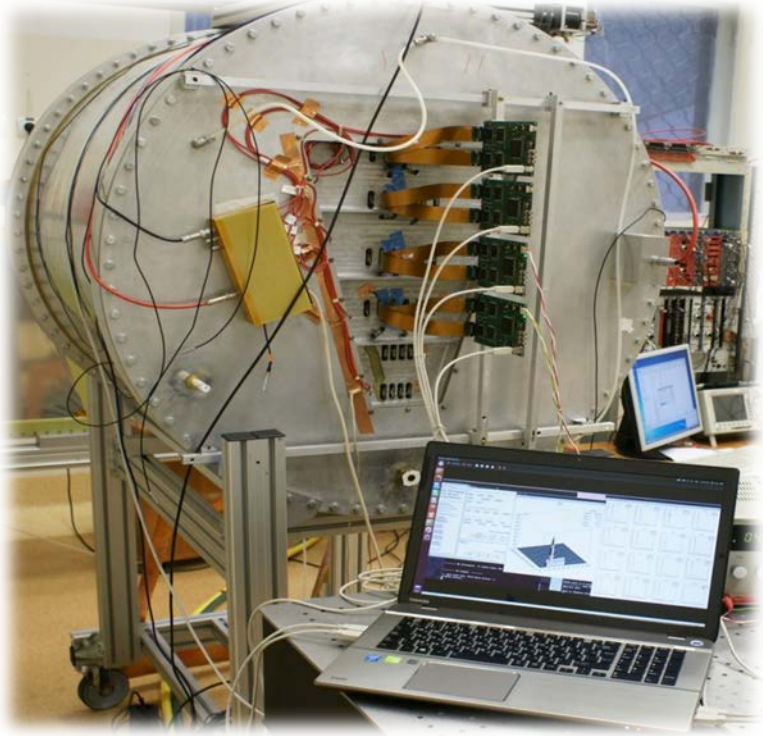
- Baseline corrections
- Tail cancellation



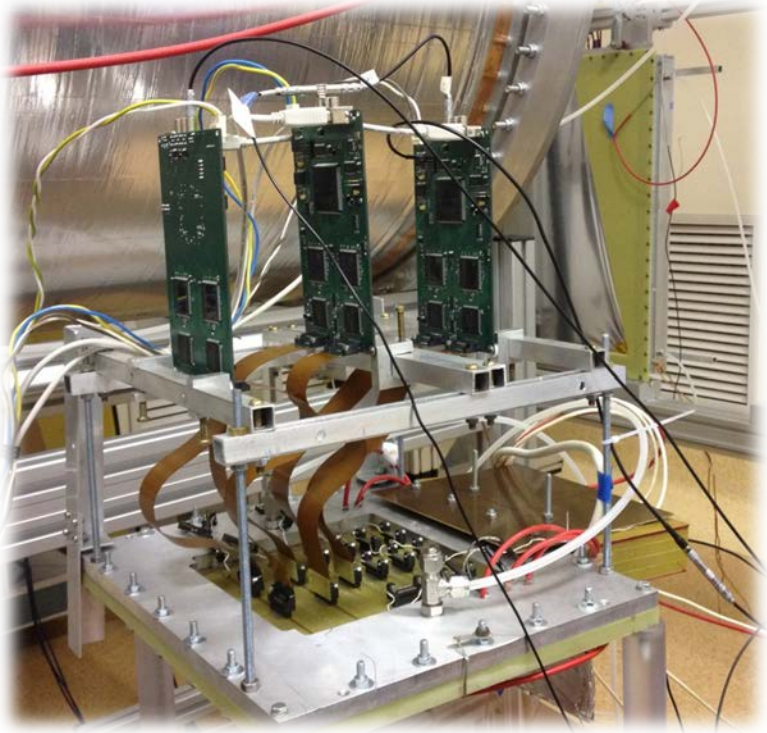
Signals prepared for zero suppression



FEE TESTING

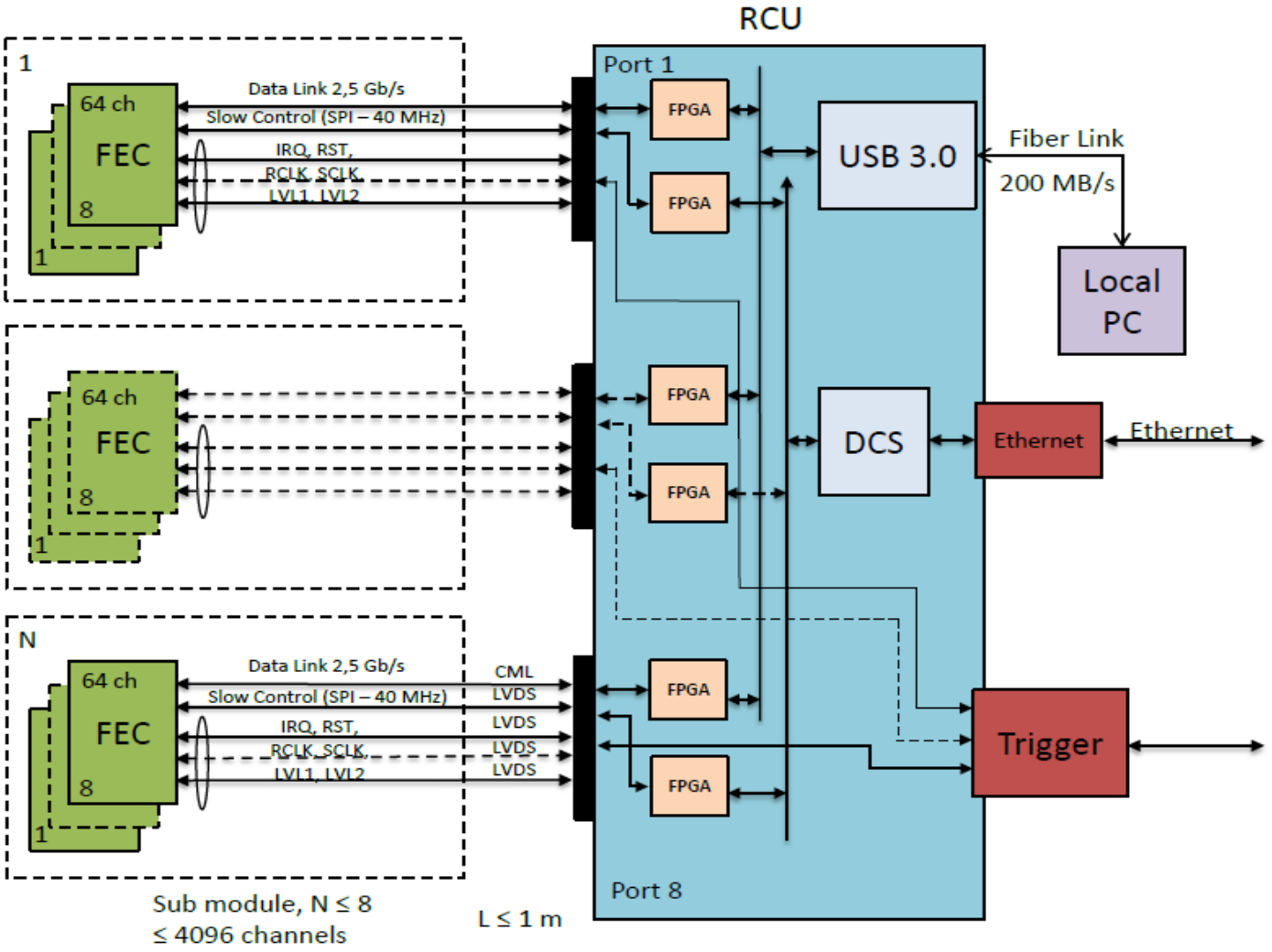


FEE on the TPC prototype

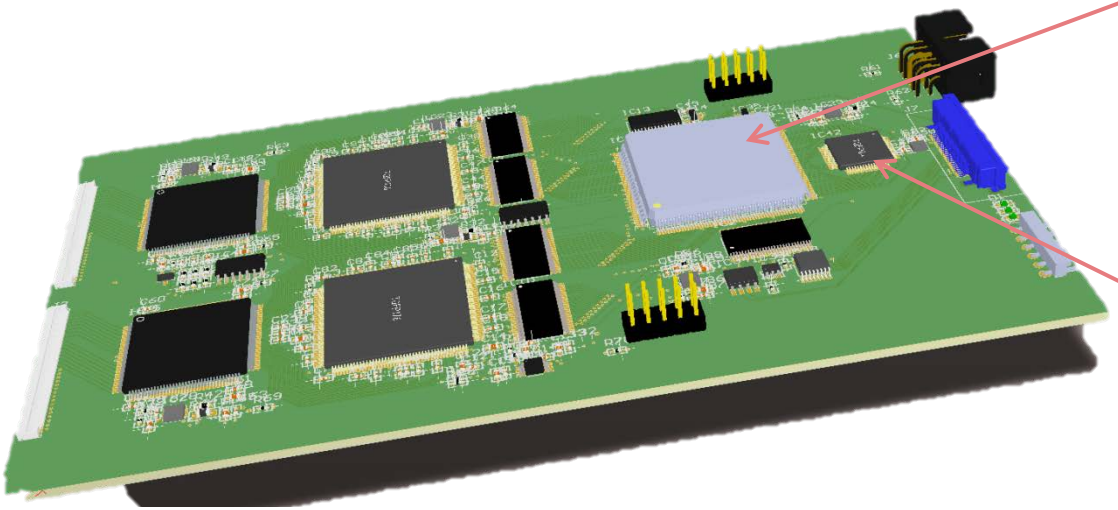


FEE on the readout chamber prototype

BLOCK DIAGRAM OF FEE BASE



NEW FEC



Microsemi FLASH technology
FPGA (more **radiation tolerance**)

Fast serial interface (SER/DES). Data throughput 2.5 Gb/s

3d-model of the new Front-End Card

- Total number of channels - **95 232**
- Total number of FECs – **1488**
- Total number of RCU - **24**

CONCLUSIONS:

- ✓ Base FEE concept was developed
- ✓ 6 Prototype card has been designed, produced & tested with developed testing software
- ✓ New FEC is almost finished
- ✓ FEE (FEC + RCU) design toward final version is ongoing

Thank you for your attention!

MAIN PARAMETERS OF THE TPC

Length of the TPC	**340 cm**
Outer radius of cylinder	**140 cm**
Inner radius of cylinder	**27 cm**
Length of the drift volume	**170cm (of each half)**
Magnetic field strength	**0.5 Tesla**
Drift gas	**90% Ar+10% CH_4**
Temperature stability	**0.5°C**
Gas amplification factor	**~ 10^4**
Number of readout chambers	**24 (12 per end plate)**
Pad size	**5x12mm^2 and 5x18mm^2**
Number of pads	**95 232**
Pad raw numbers	**53**
Maximal trigger rate	**~5 kHz**
dE/dx	**better than 8%**
$\Delta p/p$	**~ 3% in 0.1< p_t<1 GeV/c**